

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

7560 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 7560 group is the 8-bit microcomputer based on the 740 family core technology.

The 7560 group has the LCD drive control circuit, an 8-channel A-D converter, D-A converter, serial I/O and PWM as additional functions.

The various microcomputers in the 7560 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 7560 group, refer the section on group expansion.

FEATURES

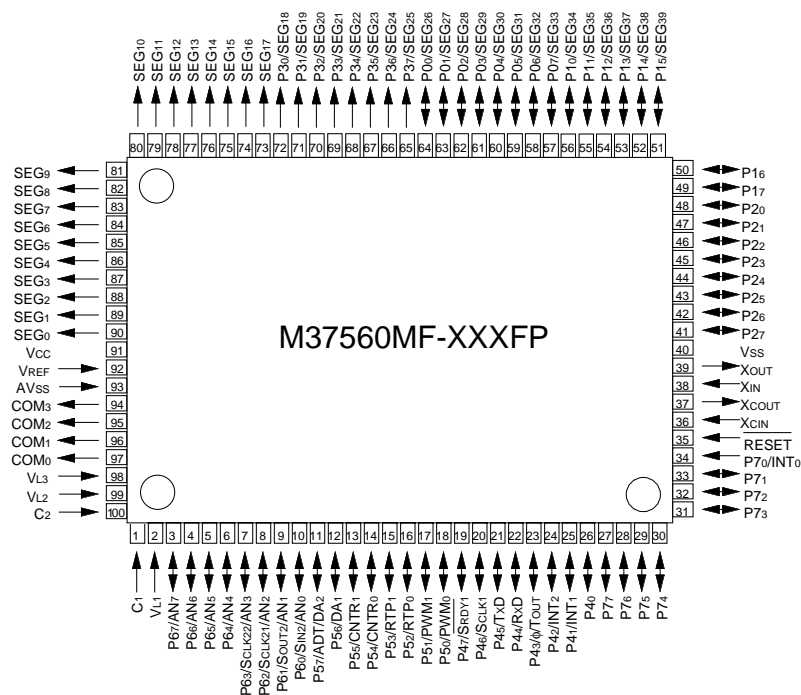
- Basic machine-language instructions 71
- The minimum instruction execution time 0.5 μ s
(at 8 MHz oscillation frequency)
- Memory size
 - ROM 32 K to 60 K bytes
 - RAM 1024 to 2560 bytes
- Programmable input/output ports 55
- Software pull-up resistors Built-in
- Output ports 8
- Input ports 1
- Interrupts 17 sources, 16 vectors
 - External 7 sources (includes key input interrupt)
 - Internal 9 sources
 - Software 1 source

- Timers 8-bit X 3, 16-bit X 2
- Serial I/O1 8-bit X 1 (UART or Clock-synchronous)
- Serial I/O2 8-bit X 1 (Clock-synchronous)
- PWM output 8-bit X 1
- A-D converter 10-bit X 8 channels
- D-A converter 8-bit X 2 channels
- LCD drive control circuit
 - Bias 1/2, 1/3
 - Duty 1/2, 1/3, 1/4
 - Common output 4
 - Segment output 40
- 2 Clock generating circuits
(connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer 14-bit X 1
- Power source voltage 2.2 to 5.5 V
(EPROM and One Time PROM version: 2.5 to 5.5 V)
(Extended operating temperature version: 3.0 to 5.5 V)
- Power dissipation
 - In high-speed mode 32 mW
(at 8 MHz oscillation frequency, at 5 V power source voltage)
 - In low-speed mode 45 μ W
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range - 20 to 85°C
(Extended operating temperature version: - 40 to 85°C)

APPLICATIONS

Camera, household appliances, consumer electronics, etc.

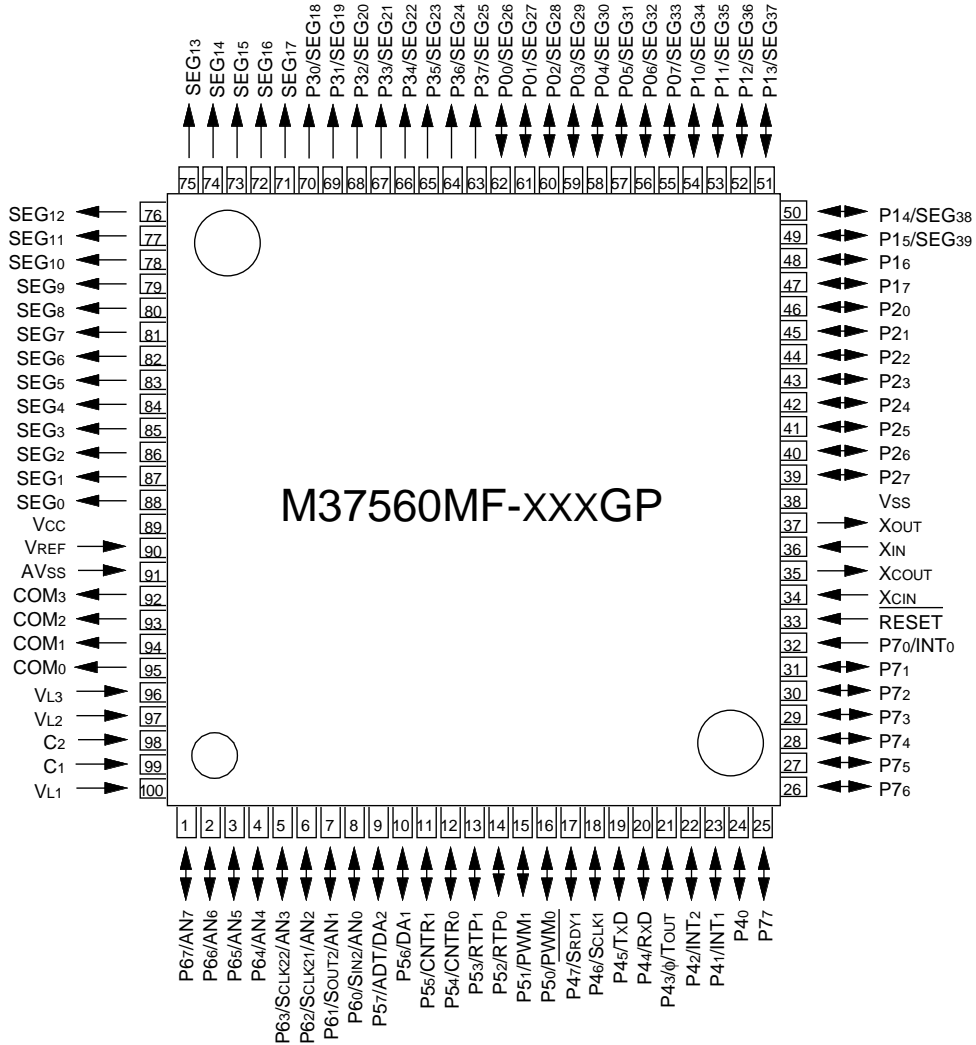
PIN CONFIGURATION (TOP VIEW)



Package type : 100P6S-A

Fig. 1 Pin configuration (Package type: 100P6S-A)

PIN CONFIGURATION (TOP VIEW)



Package type : 100P6Q-A

Fig. 2 Pin configuration (Package type: 100P6Q-A)

FUNCTIONAL BLOCK DIAGRAM (Package type: 100P6S-A)

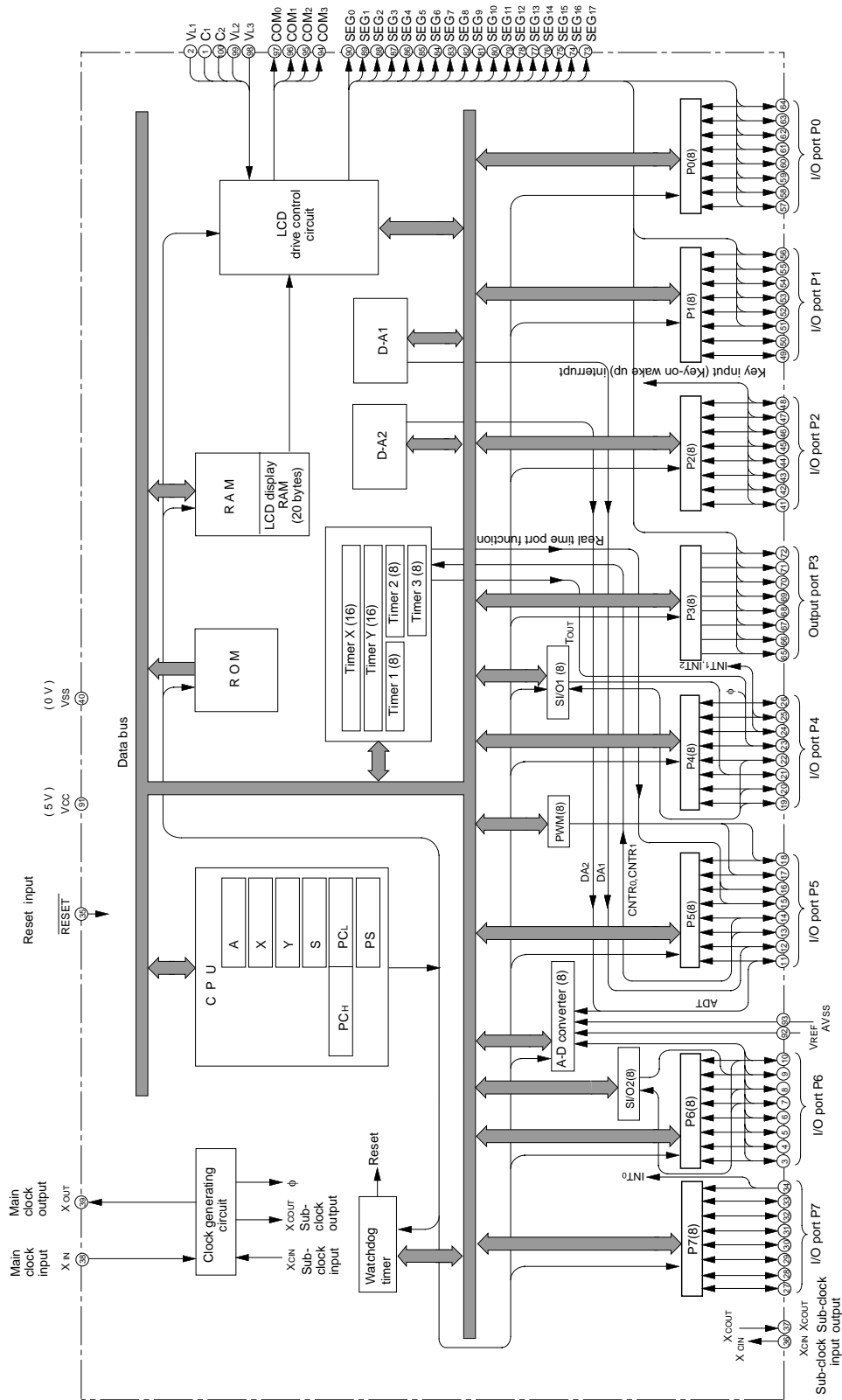


Fig. 3 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

| Pin | Name | Function | |
|---------------------------|---------------------------|--|--|
| | | | Function except a port function |
| VCC, VSS | Power source | <ul style="list-style-type: none"> •Apply voltage of 2.2 V to 5.5 V (2.5 to 5.5 V for EPROM and One Time PROM version, 3.0 to 5.5 V for extended operating temperature version) to VCC, and 0 V to VSS. | |
| VREF | Analog reference voltage | <ul style="list-style-type: none"> •Reference voltage input pin for A-D converter and D-A converter. | |
| AVSS | Analog power source | <ul style="list-style-type: none"> •GND input pin for A-D converter and D-A converter. •Connect to VSS. | |
| $\overline{\text{RESET}}$ | Reset input | <ul style="list-style-type: none"> •Reset input pin for active "L". | |
| XIN | Clock input | <ul style="list-style-type: none"> •Input and output pins for the main clock generating circuit. •Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. | |
| XOUT | Clock output | <ul style="list-style-type: none"> •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. A feedback resistor is built-in. | |
| VL1–VL3 | LCD power source | <ul style="list-style-type: none"> •Input $0 \leq VL1 \leq VL2 \leq VL3$ voltage. •Input $0 - VL3$ voltage to LCD. ($0 \leq VL1 \leq VL2 \leq VL3$ when a voltage is multiplied.) | |
| C1, C2 | Charge-pump capacitor pin | <ul style="list-style-type: none"> •External capacitor pins for a voltage multiplier (3 times) of LCD control. | |
| COM0–COM3 | Common output | <ul style="list-style-type: none"> •LCD common output pins. •COM2 and COM3 are not used at 1/2 duty ratio. •COM3 is not used at 1/3 duty ratio. | |
| SEG0–SEG17 | Segment output | <ul style="list-style-type: none"> •LCD segment output pins. | |
| P00/SEG26–P07/SEG33 | I/O port P0 | <ul style="list-style-type: none"> •8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled. •I/O direction register allows each 8-bit pin to be programmed as either input or output. | <ul style="list-style-type: none"> •LCD segment output pins |
| P10/SEG34–P15/SEG39 | I/O port P1 | <ul style="list-style-type: none"> •6-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled. •I/O direction register allows each 6-bit pin to be programmed as either input or output. | |
| P16, P17 | | <ul style="list-style-type: none"> •2-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled. | |
| P20 – P27 | I/O port P2 | <ul style="list-style-type: none"> •8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled. | <ul style="list-style-type: none"> •Key input (key-on wake-up) interrupt input pins |
| P30/SEG18 – P37/SEG25 | Output port P3 | <ul style="list-style-type: none"> •8-bit output. •CMOS 3-state output structure. •Port output control is enabled. | <ul style="list-style-type: none"> •LCD segment output pins |

Table 2 Pin description (2)

| Pin | Name | Function | Function except a port function |
|--|------------------|--|---|
| | | | |
| P40 | I/O port P4 | <ul style="list-style-type: none"> •1-bit I/O port. •CMOS compatible input level. •N-channel open-drain output structure. •I/O direction register allows this pin to be individually programmed as either input or output. | |
| P41/INT1, P42/INT2 | | | •INTi interrupt input pins |
| P43/φ/TOUT | | | <ul style="list-style-type: none"> •System clock φ output pin •Timer 2 output pin |
| P44/RxD, P45/TxD, P46/SCLK1, P47/SRDY1 | | | •Serial I/O1 I/O pins |
| P50/PWM0, P51/PWM1 | I/O port P5 | <ul style="list-style-type: none"> •8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled. | •PWM output pins |
| P52/RTP0, P53/RTP1 | | | •Real time port output pins |
| P54/CNTR0, P55/CNTR1 | | | •Timer X, Y I/O pins |
| P56/DA1 | | | •D-A converter output pin |
| P57/ADT/DA2 | | | •D-A converter output pin •A-D external trigger input pin |
| P60/SIN2/AN0, P61/SOUT2/AN1, P62/SCLK21/AN2, P63/SCLK22/AN3 | I/O port P6 | <ul style="list-style-type: none"> •8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled. | •A-D converter input pins •Serial I/O2 I/O pins |
| P64/AN4– P67/AN7 | | | •A-D converter input pins |
| P70/INT0 | Input port P7 | •1-bit input port. | •INT0 interrupt input pin |
| P71–P77 | I/O port P7 | <ul style="list-style-type: none"> •7-bit I/O port. •CMOS compatible input level. •N-channel open-drain output structure. •I/O direction register allows each pin to be individually programmed as either input or output. | |
| XCOUT | Sub-clock output | <ul style="list-style-type: none"> •Sub-clock generating circuit I/O pins. (Connect a oscillator. External clock cannot be used.) | |
| XCIN | Sub-clock input | | |

PART NUMBERING

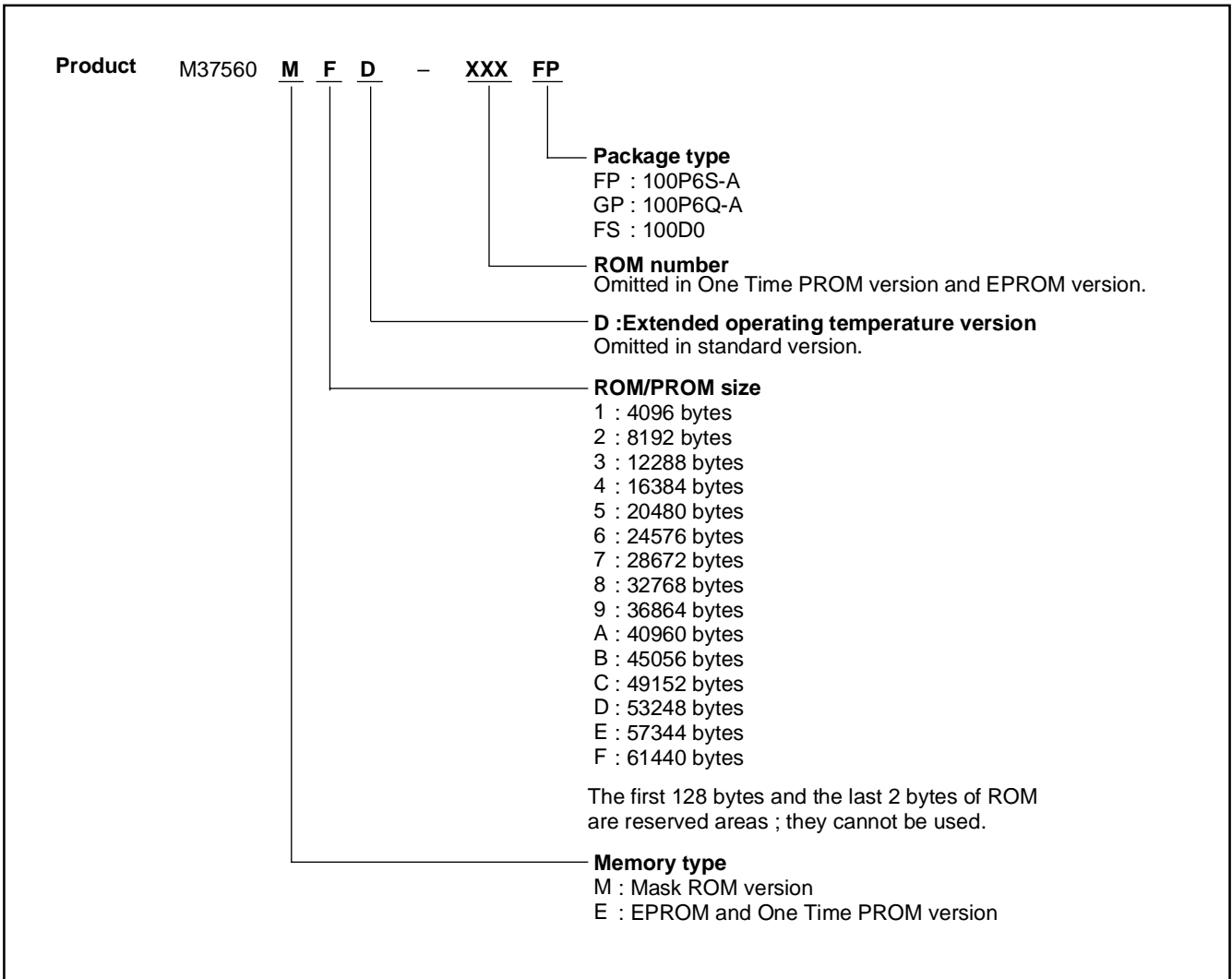


Fig. 4 Part numbering

GROUP EXPANSION

Mitsubishi expands the 7560 group as follows.

Memory Type

Support for mask ROM version.

Memory Size

ROM size 32 K to 60 K bytes
 RAM size 1024 to 2560 bytes

Packages

100P6Q-A 0.5 mm-pitch plastic molded QFP
 100P6S-A 0.65 mm-pitch plastic molded QFP

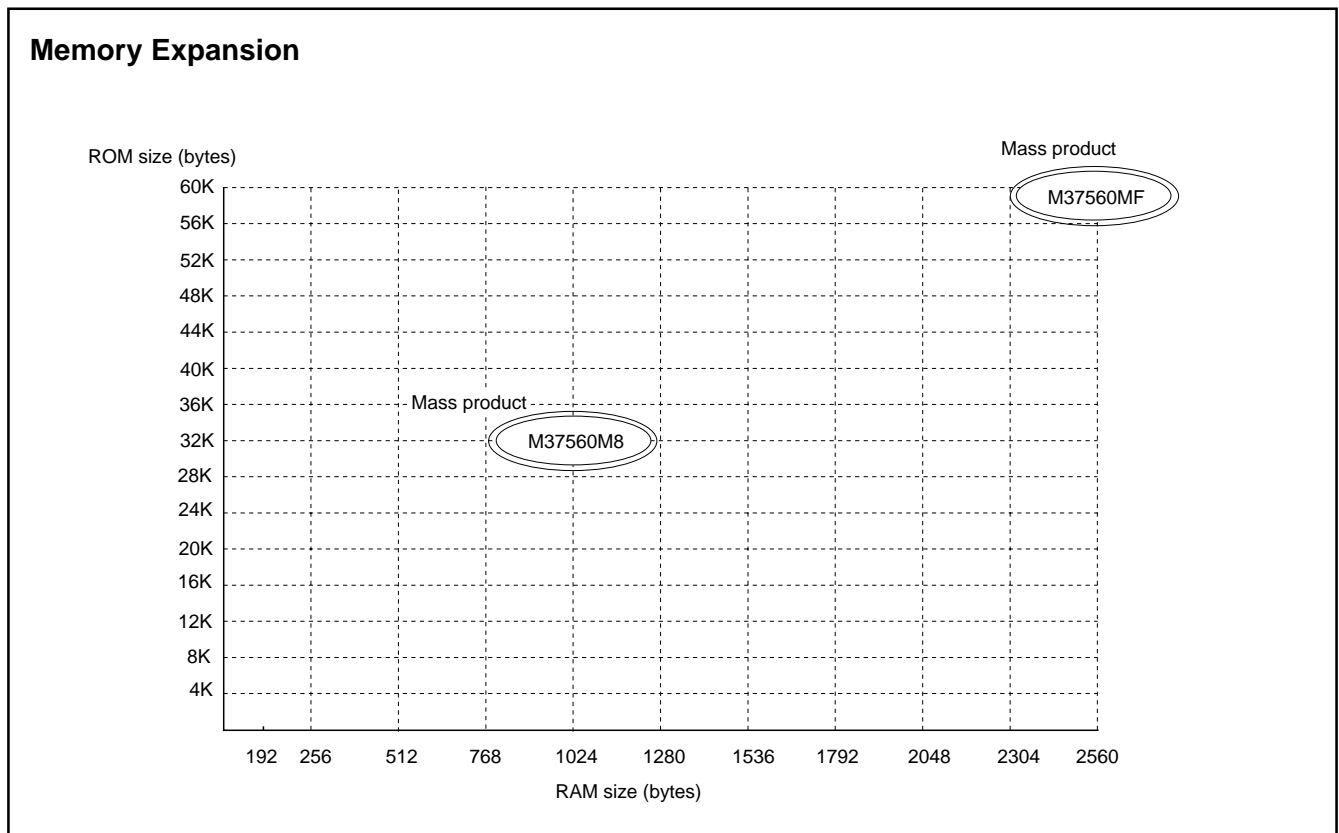


Fig. 5 Memory expansion

Currently products are listed below.

Table 3 List of products

As of Jan. 2003

| Product | ROM size (bytes) ROM size for User in () | RAM size (bytes) | Package | Remarks |
|-----------------|--|------------------|----------|------------------|
| M37560M8-XXXXFP | 32768 (32638) | 1024 | 100P6S-A | Mask ROM version |
| M37560M8-XXXXGP | | | 100P6Q-A | Mask ROM version |
| M37560MF-XXXXFP | 61440 (61310) | 2560 | 100P6S-A | Mask ROM version |
| M37560MF-XXXXGP | | | 100P6Q-A | Mask ROM version |

**GROUP EXPANSION
(One Time and EPROM version)**

Mitsubishi expands the 7560 group as follows.

Memory Type

Support for One Time and EPROM version.

Memory Size

ROM size 60 K bytes

RAM size 2560 bytes

Packages

100P6Q-A 0.5 mm-pitch plastic molded QFP

100P6S-A 0.65 mm-pitch plastic molded QFP

100D0 Ceramic LCC (EPROM version)

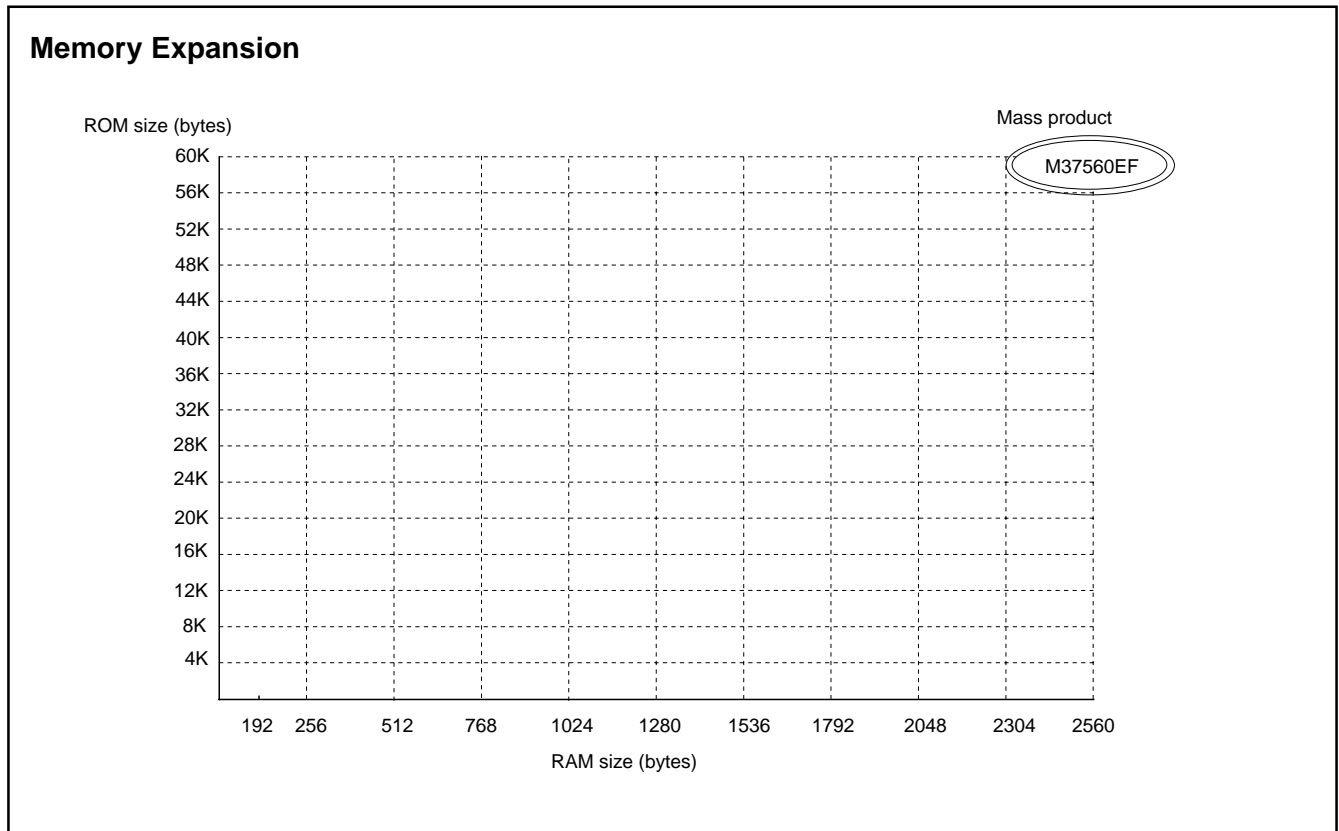


Fig. 6 Memory expansion

Currently products are listed below.

Table 4 List of products

As of Jan. 2003

| Product | ROM size (bytes) ROM size for User in () | RAM size (bytes) | Package | Remarks |
|------------|--|------------------|----------|-----------------------|
| M37560EFP | 61440 (61310) | 2560 | 100P6S-A | One Time PROM version |
| M37560EFGP | | | 100P6Q-A | One Time PROM version |
| M37560EFFS | | | 100D0 | EPROM version |

**GROUP EXPANSION
(Extended operating temperature version)**

Mitsubishi expands the 7560 group as follows.

Packages

100P6S-A 0.65 mm-pitch plastic molded QFP

Memory Type

Support for extended operating temperature version.

Memory Size

ROM size 60 K bytes

RAM size 2560 bytes

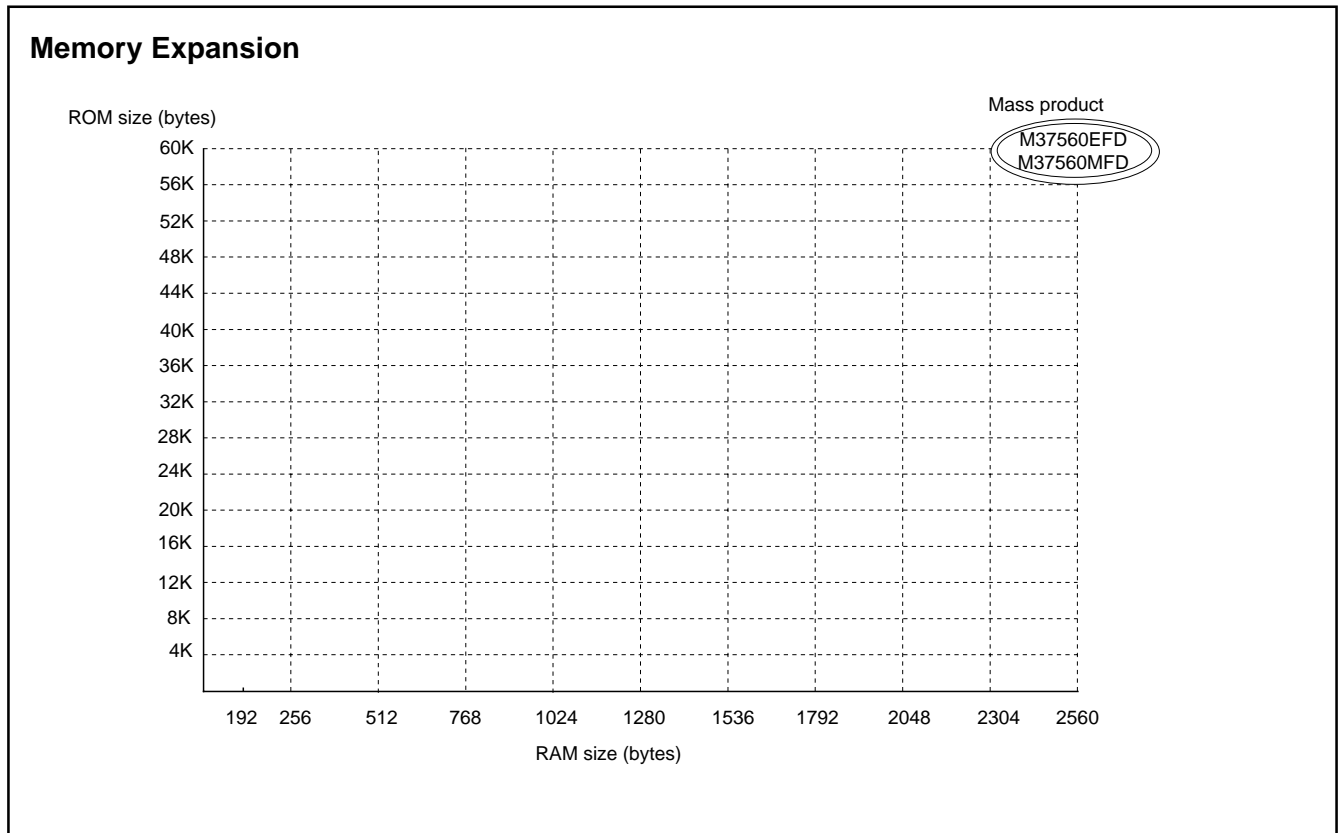


Fig. 7 Memory expansion

Currently products are listed below.

Table 5 List of products

As of Jan. 2003

| Product | ROM size (bytes) ROM size for User in () | RAM size (bytes) | Package | Remarks |
|------------------|--|------------------|----------|---|
| M37560MFD-XXXXFP | 61440 (61310) | 2560 | 100P6S-A | Mask ROM version (Extended operating temperature version) |
| M37560EFD-XXXXFP | | | | One Time PROM version (Extended operating temperature version) |

**FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)**

The 7560 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

The central processing unit (CPU) has six registers. Figure 8 shows the 740 Family CPU register structure.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as arithmetic data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

Figure 9 shows the operations of pushing register contents onto the stack and popping them from the stack. Table 6 shows the push and pop instructions of accumulator or processor status register.

Store registers other than those described in Figure 9 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

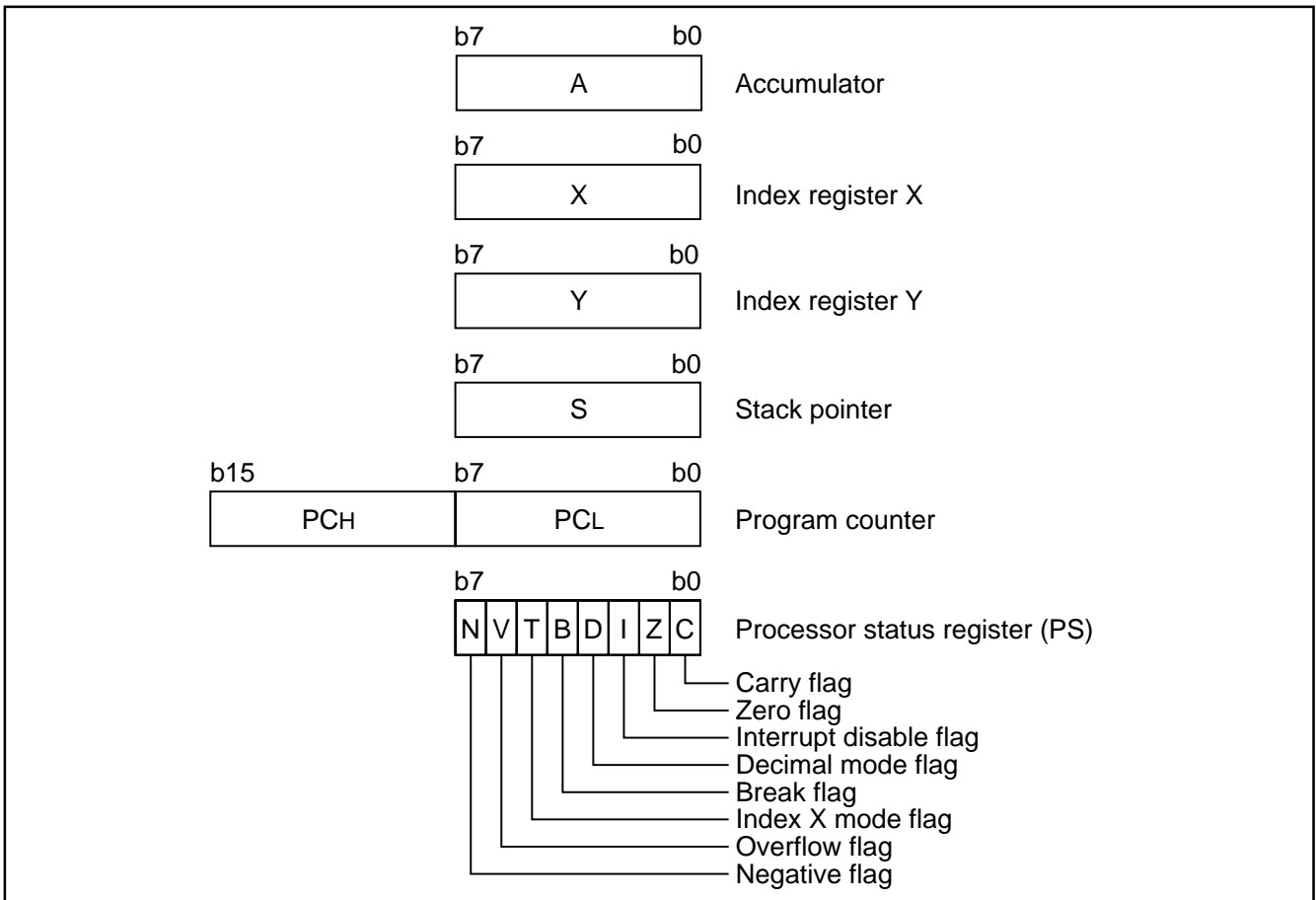


Fig. 8 740 Family CPU register structure

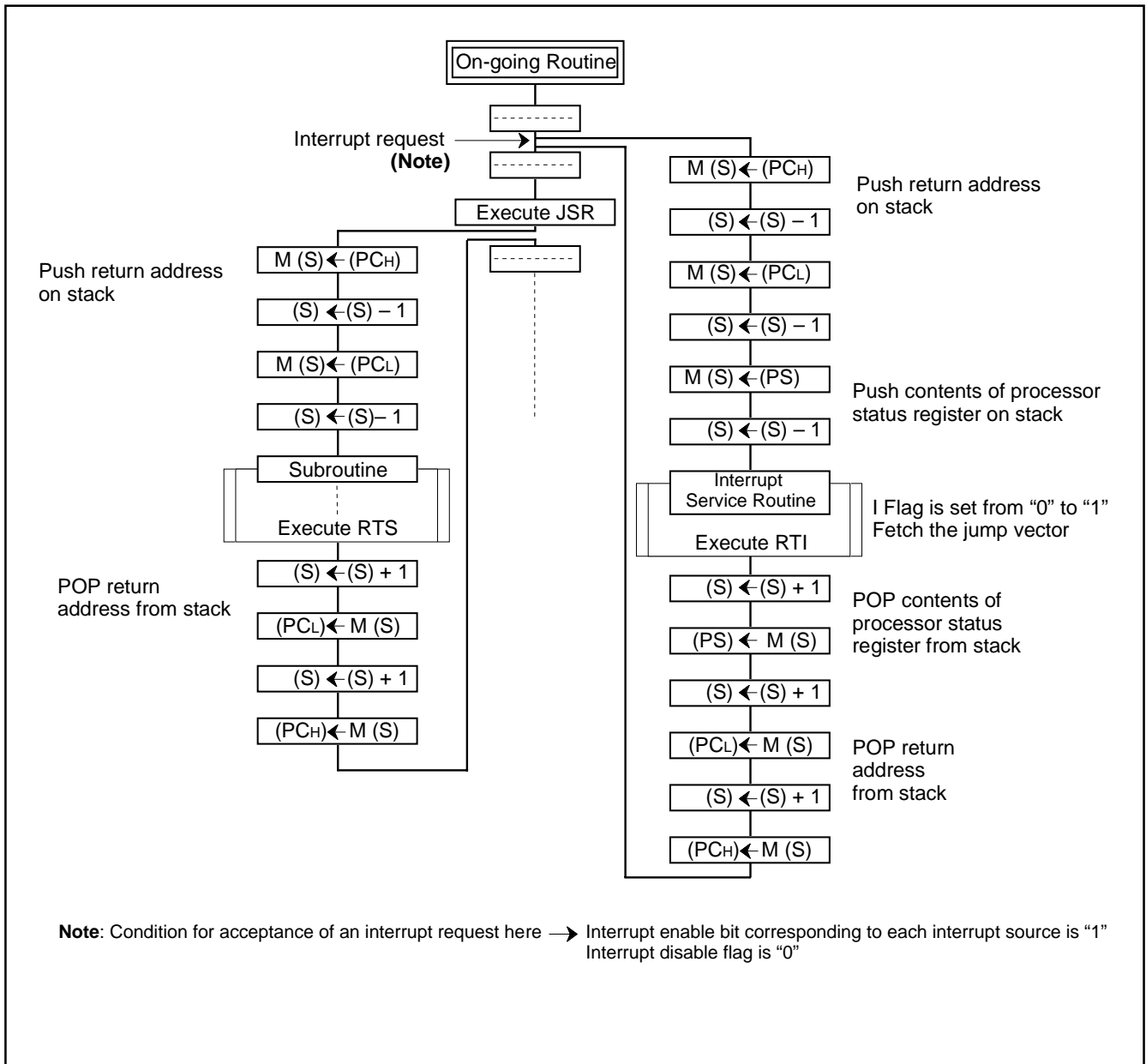


Fig. 9 Register push and pop at interrupt generation and subroutine call

Table 6 Push and pop instructions of accumulator or processor status register

| | Push instruction to stack | Pop instruction from stack |
|---------------------------|---------------------------|----------------------------|
| Accumulator | PHA | PLA |
| Processor status register | PHP | PLP |

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

- Bit 1: Zero flag (Z)

The Z flag is set to "1" if the result of an immediate arithmetic operation or a data transfer is "0", and set to "0" if the result is anything other than "0".

- Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

- Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

- Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. When the BRK instruction is generated, the B flag is set to "1" automatically. When the other interrupts are generated, the B flag is set to "0", and the processor status register is pushed onto the stack.

- Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

- Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set to "1" if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the V flag.

- Bit 7: Negative flag (N)

The N flag is set to "1" if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 7 Instructions to set each bit of processor status register to "0" or "1"

| | C flag | Z flag | I flag | D flag | B flag | T flag | V flag | N flag |
|----------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Instruction setting to "1" | SEC | – | SEI | SED | – | SET | – | – |
| Instruction setting to "0" | CLC | – | CLI | CLD | – | CLT | CLV | – |

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the system clock control bits, etc.

The CPU mode register is allocated at address 003B16.

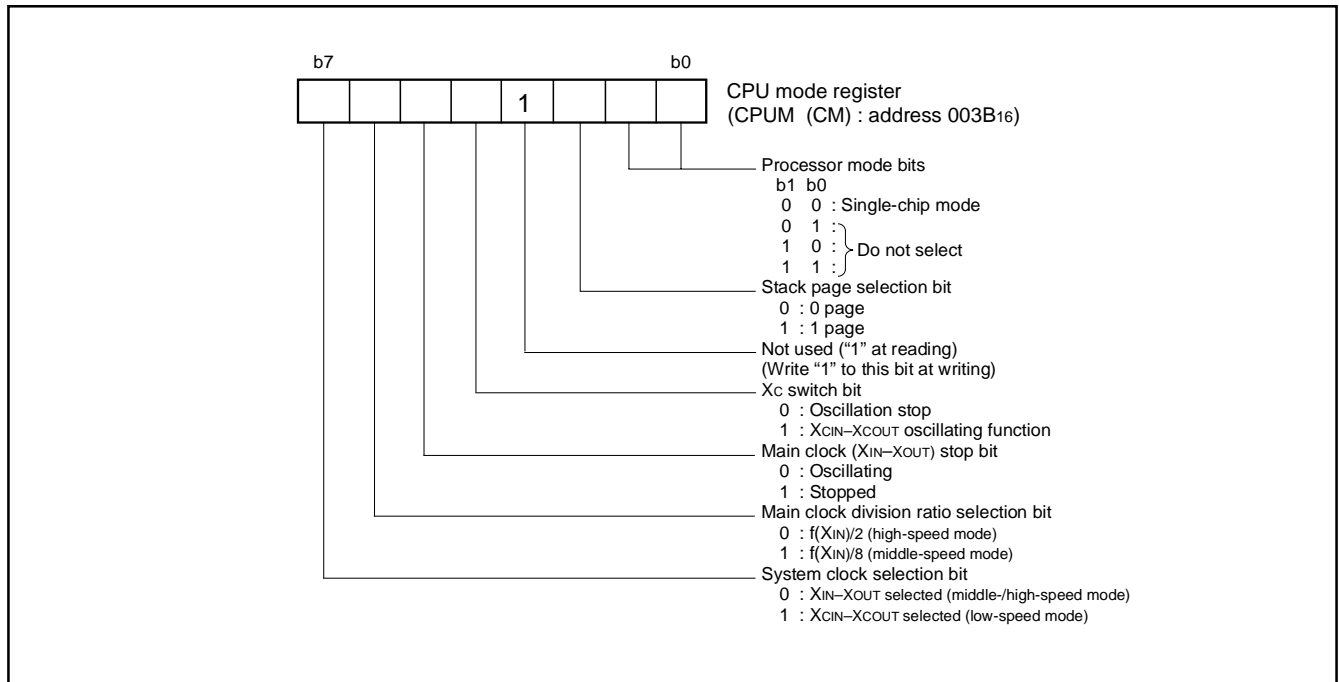


Fig. 10 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

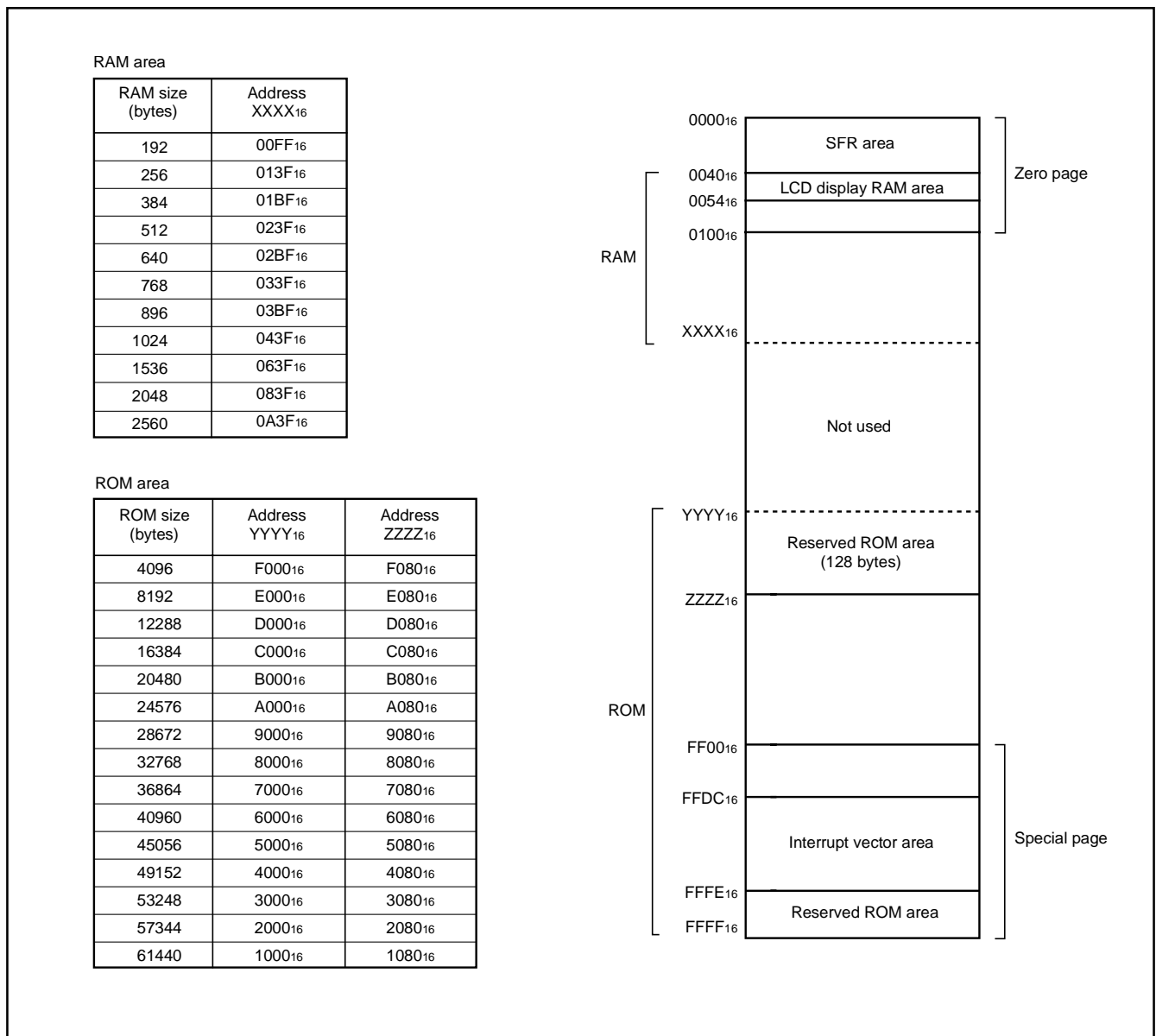


Fig. 11 Memory map diagram

| | | | |
|--------------------|---|--------------------|---|
| 0000 ¹⁶ | Port P0 register (P0) | 0020 ¹⁶ | Timer X low-order register (TXL) |
| 0001 ¹⁶ | Port P0 direction register (P0D) | 0021 ¹⁶ | Timer X high-order register (TXH) |
| 0002 ¹⁶ | Port P1 register (P1) | 0022 ¹⁶ | Timer Y low-order register (TYL) |
| 0003 ¹⁶ | Port P1 direction register (P1D) | 0023 ¹⁶ | Timer Y high-order register (TYH) |
| 0004 ¹⁶ | Port P2 register (P2) | 0024 ¹⁶ | Timer 1 register (T1) |
| 0005 ¹⁶ | Port P2 direction register (P2D) | 0025 ¹⁶ | Timer 2 register (T2) |
| 0006 ¹⁶ | Port P3 register (P3) | 0026 ¹⁶ | Timer 3 register (T3) |
| 0007 ¹⁶ | Port P3 output control register (P3C) | 0027 ¹⁶ | Timer X mode register (TXM) |
| 0008 ¹⁶ | Port P4 register (P4) | 0028 ¹⁶ | Timer Y mode register (TYM) |
| 0009 ¹⁶ | Port P4 direction register (P4D) | 0029 ¹⁶ | Timer 123 mode register (T123M) |
| 000A ¹⁶ | Port P5 register (P5) | 002A ¹⁶ | TOU/φ output control register (CKOUT) |
| 000B ¹⁶ | Port P5 direction register (P5D) | 002B ¹⁶ | PWM control register (PWMCON) |
| 000C ¹⁶ | Port P6 register (P6) | 002C ¹⁶ | PWM prescaler (PREPWM) |
| 000D ¹⁶ | Port P6 direction register (P6D) | 002D ¹⁶ | PWM register (PWM) |
| 000E ¹⁶ | Port P7 register (P7) | 002E ¹⁶ | Reserved area (Note) |
| 000F ¹⁶ | Port P7 direction register (P7D) | 002F ¹⁶ | Reserved area (Note) |
| 0010 ¹⁶ | | 0030 ¹⁶ | Reserved area (Note) |
| 0011 ¹⁶ | | 0031 ¹⁶ | Reserved area (Note) |
| 0012 ¹⁶ | | 0032 ¹⁶ | D-A1 conversion register (DA1) |
| 0013 ¹⁶ | | 0033 ¹⁶ | D-A2 conversion register (DA2) |
| 0014 ¹⁶ | A-D conversion low-order register (ADL) | 0034 ¹⁶ | A-D control register (ADCON) |
| 0015 ¹⁶ | Key input control register (KIC) | 0035 ¹⁶ | A-D conversion high-order register (ADH) |
| 0016 ¹⁶ | PULL register A (PULLA) | 0036 ¹⁶ | D-A control register (DACON) |
| 0017 ¹⁶ | PULL register B (PULLB) | 0037 ¹⁶ | Watchdog timer control register (WDTCON) |
| 0018 ¹⁶ | Transmit/Receive buffer register(TB/RB) | 0038 ¹⁶ | Segment output enable register (SEG) |
| 0019 ¹⁶ | Serial I/O1 status register (SIO1STS) | 0039 ¹⁶ | LCD mode register (LM) |
| 001A ¹⁶ | Serial I/O1 control register (SIO1CON) | 003A ¹⁶ | Interrupt edge selection register (INTEDGE) |
| 001B ¹⁶ | UART control register (UARTCON) | 003B ¹⁶ | CPU mode register (CPUM) |
| 001C ¹⁶ | Baud rate generator (BRG) | 003C ¹⁶ | Interrupt request register 1(IREQ1) |
| 001D ¹⁶ | Serial I/O2 control register (SIO2CON) | 003D ¹⁶ | Interrupt request register 2(IREQ2) |
| 001E ¹⁶ | Reserved area (Note) | 003E ¹⁶ | Interrupt control register 1(ICON1) |
| 001F ¹⁶ | Serial I/O2 register (SIO2) | 003F ¹⁶ | Interrupt control register 2(ICON2) |

Note: Do not write to the addresses of reserved area.

Fig. 12 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The I/O ports (ports P0, P1, P2, P4, P5, P6, P71–P77) have direction registers. Ports P16, P17, P4, P5, P6, and P71–P77 can be set to input mode or output mode by each pin individually. P00–P07 and P10–P15 are respectively set to input mode or output mode in a lump by bit 0 of the direction registers of ports P0 and P1 (see Figure 13).

When “0” is set to the bit corresponding to a pin, that pin becomes an input mode. When “1” is set to that bit, that pin becomes an output mode.

If data is read from a port set to output mode, the value of the port latch is read, not the value of the pin itself. A port set to input mode is floating. If data is read from a port set to input mode, the value of the pin itself is read. If a pin set to input mode is written to, only the port latch is written to and the pin remains floating.

Port P3 Output Control Register

Bit 0 of the port P3 output control register (address 0007₁₆) enables control of the output of ports P30–P37.

When the bit is set to “1”, the port output function is valid.

When resetting, bit 0 of the port P3 output control register is set to “0” (the port output function is invalid) and pulled up.

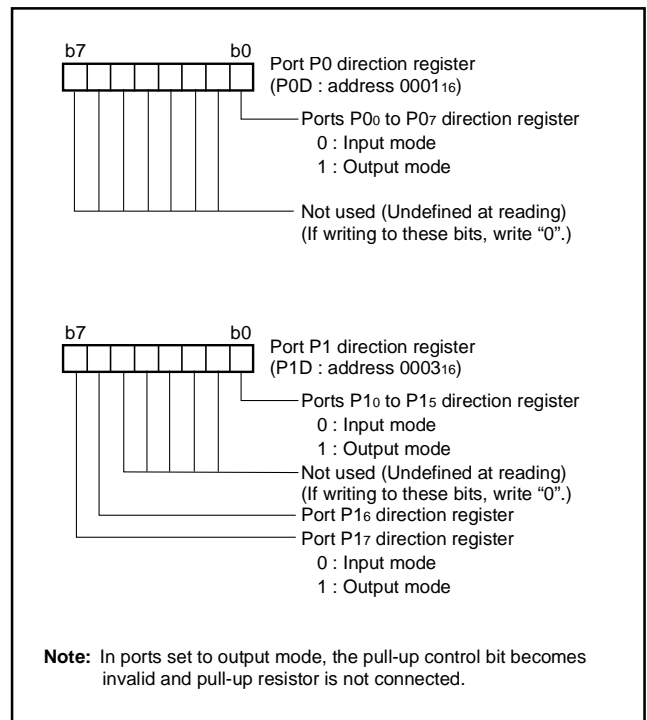


Fig. 13 Structure of port P0 direction register, port P1 direction register

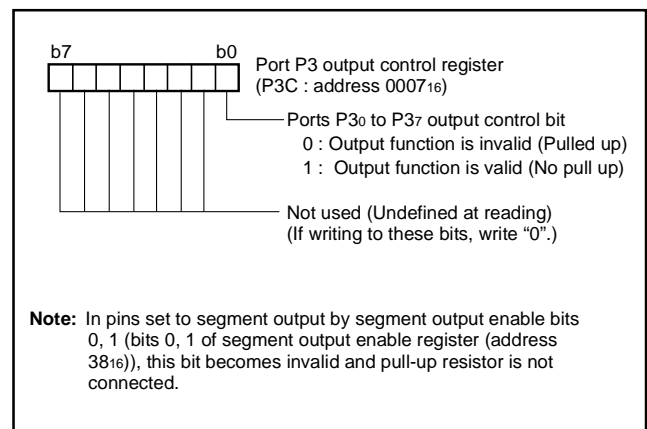


Fig. 14 Structure of port P3 output control register

Pull-up Control

By setting the PULL register A (address 0016₁₆) or the PULL register B (address 0017₁₆), ports P0 to P2, P4 to P6 can control pull-up with a program.

However, the contents of PULL register A and PULL register B do not affect ports set to output mode and the ports are not pulled up. The PULL register A setting is invalid for pins selecting segment output with the segment output enable register and the pins are not pulled up.

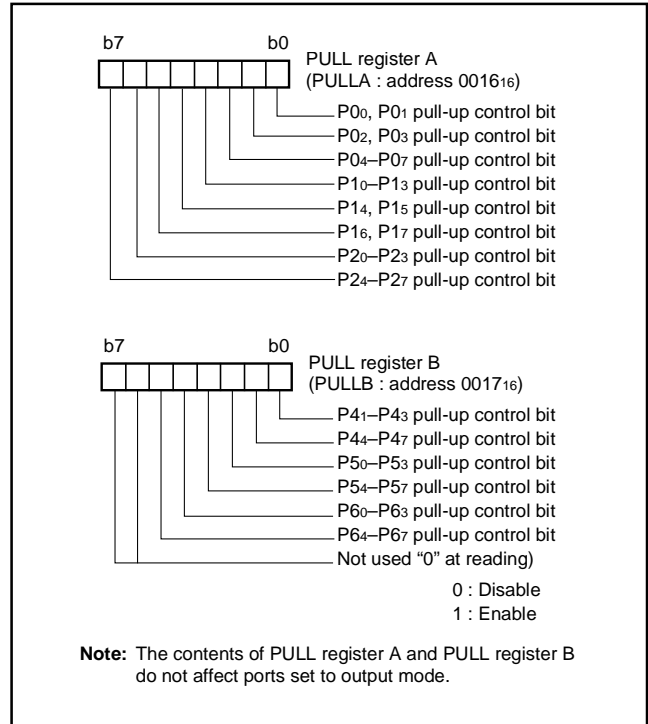


Fig. 15 Structure of PULL register A and PULL register B

Table 8 List of I/O port function (1)

| Pin | Name | Input/Output | I/O Format | Non-Port Function | Related SFRs | Diagram No. | | |
|---|---------|----------------------------------|--|--|---|---|---|-----|
| P00/SEG26– P07/SEG33 | Port P0 | Input/output, byte unit | CMOS compatible input level CMOS 3-state output | LCD segment output | PULL register A Segment output enable register | (1) (2) | | |
| P10/SEG34– P15/SEG39 | Port P1 | Input/output, 6-bit unit | CMOS compatible input level CMOS 3-state output | LCD segment output | PULL register A Segment output enable register | (1) (2) | | |
| P16 , P17 | | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | | PULL register A | (4) | | |
| P20–P27 | Port P2 | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | Key input (key-on wake-up) interrupt input | PULL register A Interrupt control register 2 Key input control register | | | |
| P30/SEG18– P37/SEG25 | Port P3 | Output | CMOS 3-state output | LCD segment output | Segment output enable register Port P3 output control register | (3) | | |
| P40 | Port P4 | Input/output, individual bits | CMOS compatible input level N-channel open-drain output | | | (13) | | |
| P41/INT1, P42/INT2 | | | | CMOS compatible input level | INTi interrupt input | Interrupt edge selection register | (4) | |
| P43/φ/TOUT | | | | CMOS 3-state output | Timer 2 output System clock φ output | PULL register B Timer 123 mode register TOUT/φ output control register | (12) | |
| P44/RxD, P45/TxD, P46/SCLK1, P47/SRDY1 | | | | Serial I/O1 I/O | | | PULL register B Serial I/O1 control register Serial I/O1 status register UART control register | (5) |
| | | | | | | | | (6) |
| | | | | | (7) | | | |
| | | | | | (8) | | | |
| P50/PWM0, P51/PWM1 | Port P5 | Input/output, individual bits | CMOS compatible input level CMOS 3-state output | PWM output | PULL register B PWM control register | (10) | | |
| P52/RTP0, P53/RTP1 | | | | Real time port output | PULL register B Timer X mode register | (9) | | |
| P54/CNTR0 | | | | Timer X I/O | PULL register B Timer X mode register | (11) | | |
| P55/CNTR1 | | | | Timer Y input | PULL register B Timer Y mode register | (14) | | |
| P56/DA1 | | | | DA1 output | PULL register B D-A control register | (15) | | |
| P57/ADT/ DA2 | | | | DA2 output A-D external trigger input | PULL register B D-A control register A-D control register | (15) | | |
| | | | | | | | | |

Table 9 List of I/O port function (2)

| Pin | Name | Input/Output | I/O Format | Non-Port Function | Related SFRs | Diagram No. |
|---------------------|---------|---|--|--|--|-------------|
| P60/SIN2/AN0 | Port P6 | Input/ output, individual bits | CMOS compatible input level CMOS 3-state output | A-D converter input Serial I/O2 I/O | PULL register B A-D control register Serial I/O2 control register | (17) |
| P61/SOUT2/ AN1 | | | | | | (18) |
| P62/SCLK21/ AN2 | | | | | | (19) |
| P63/SCLK22 / AN3 | | | | | | (20) |
| P64/AN4– P67/AN7 | | | | A-D converter input | A-D control register PULL register B | (16) |
| P70/INT0 | Port P7 | Input | CMOS compatible input level | INT0 interrupt input | Interrupt edge selection register | (23) |
| P71–P77 | | Input/ output, individual bits | CMOS compatible input level N-channel open-drain output | | | (13) |
| COM0–COM3 | Common | Output | LCD common output | | LCD mode register | (21) |
| SEG0–SEG17 | Segment | Output | LCD segment output | | | (22) |

Notes 1: How to use double-function ports as function I/O pins, refer to the applicable sections.

2: Make sure that the input level at each pin is either 0 V or VCC before execution of the STP instruction. When an electric potential is at an intermediate potential, a current will flow from VCC to VSS through the input-stage gate and power source current may increase.

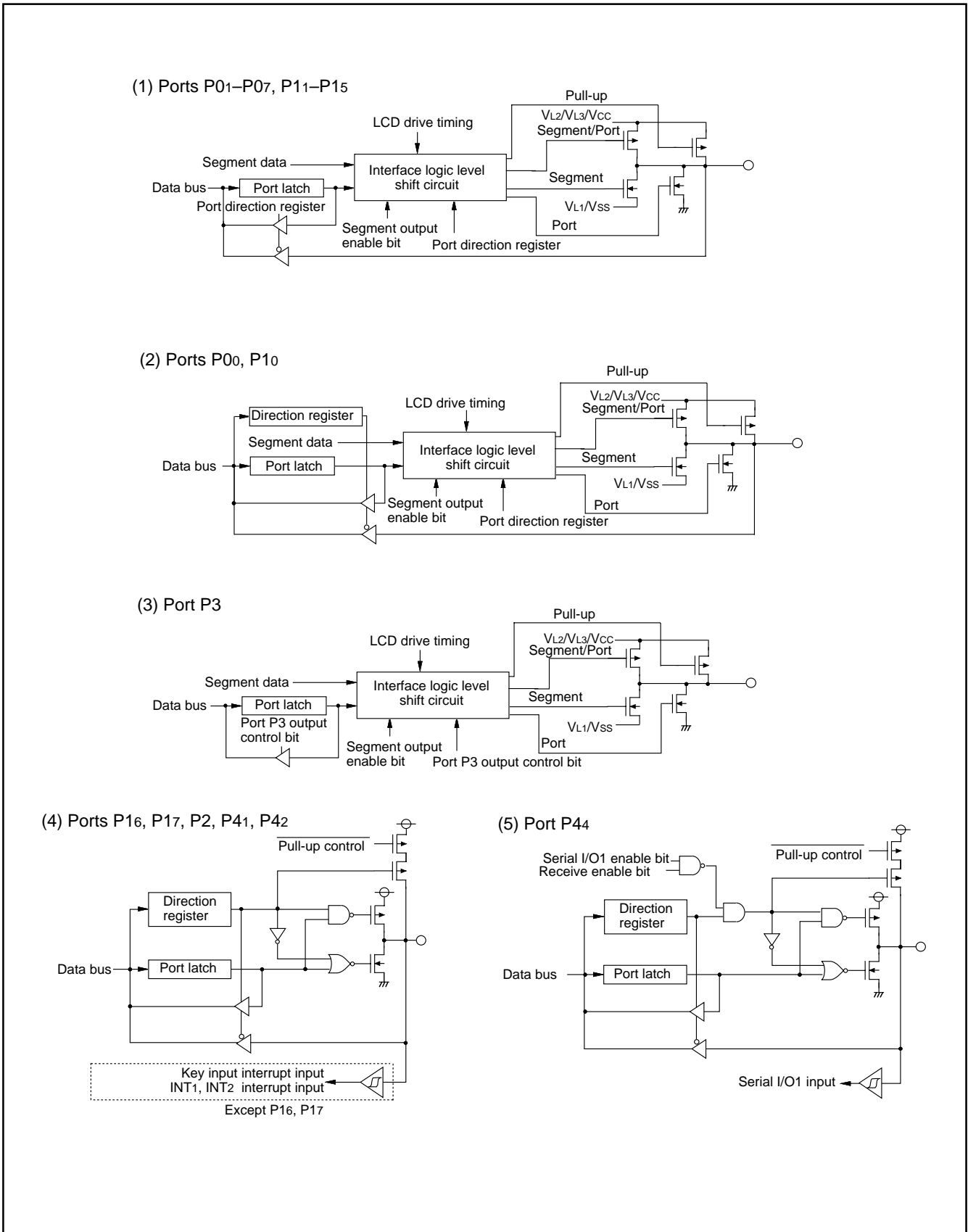


Fig. 16 Port block diagram (1)

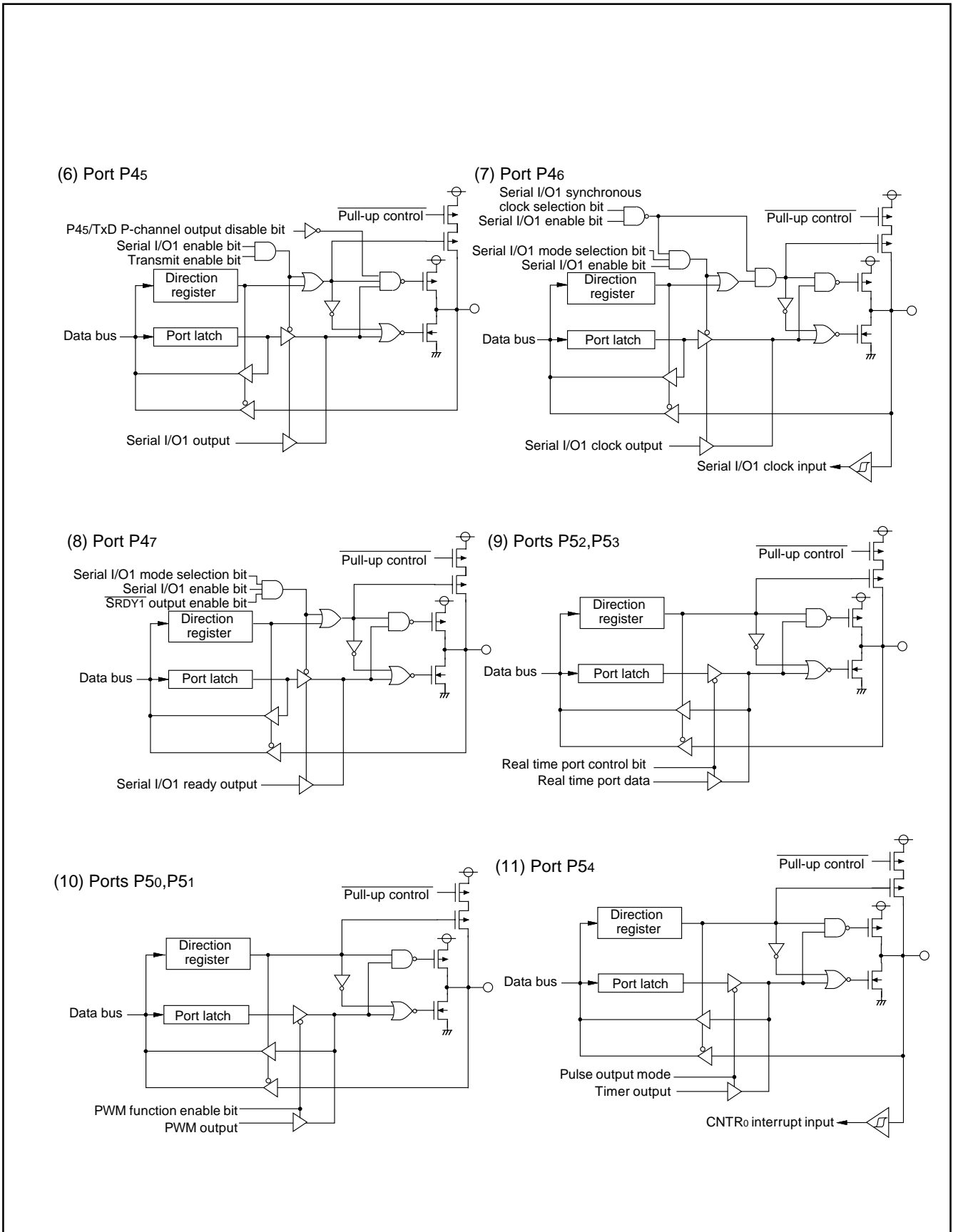


Fig. 17 Port block diagram (2)

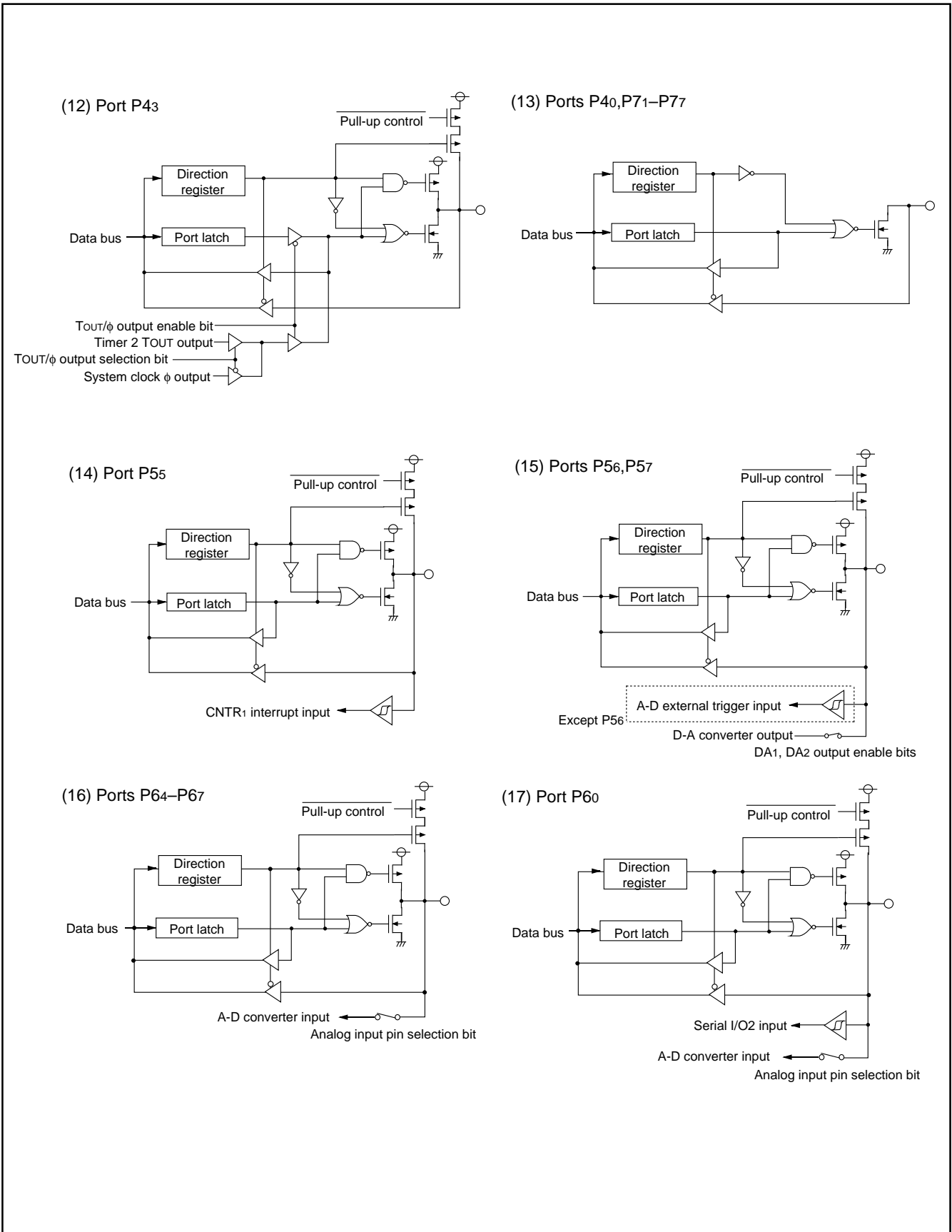


Fig. 18 Port block diagram (3)

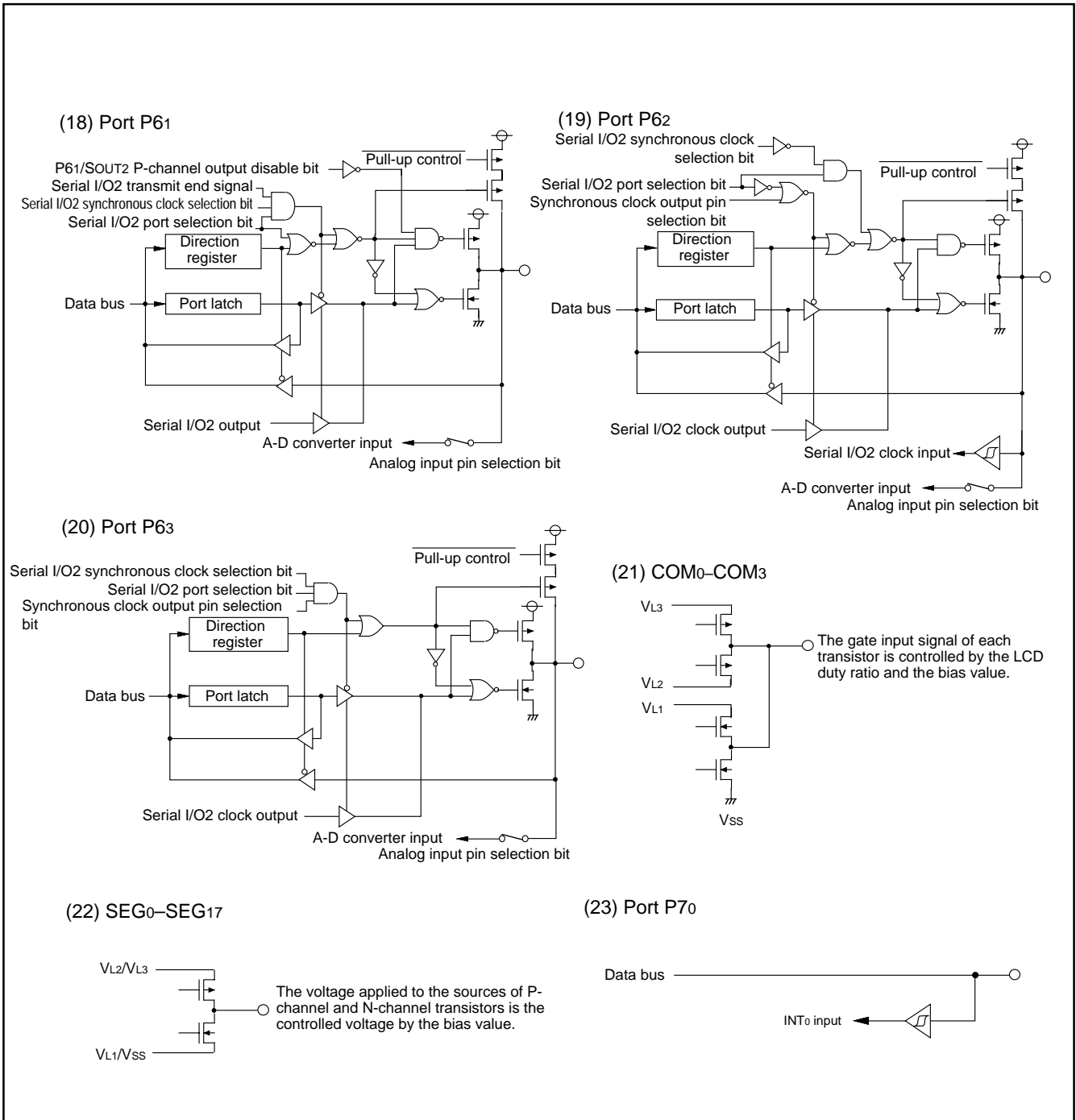


Fig. 19 Port block diagram (4)

INTERRUPTS

Interrupts occur by seventeen sources: seven external, nine internal, and one software. When an interrupt request is accepted, the program branches to the interrupt jump destination address set in the vector address (see Figure 10).

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt is accepted if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set to "0" or "1" by program.

Interrupt request bits can be set to "0" by program, but cannot be set to "1" by program.

The BRK instruction interrupt and reset cannot be disabled with any flag or bit. When the interrupt disable (I) flag is set to "1", all interrupt requests except the BRK instruction interrupt and reset are not accepted.

When several interrupt requests occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt jump destination address is read from the vector table into the program counter.
3. The interrupt disable flag is set to "1" and the corresponding interrupt request bit is set to "0".

Table 10 Interrupt vector addresses and priority

| Interrupt Source | Priority | Vector Addresses (Note 1) | | Interrupt Request Generating Conditions | Remarks |
|----------------------------|----------|---------------------------|--------------------|--|---|
| | | High | Low | | |
| Reset (Note 2) | 1 | FFFD ₁₆ | FFFC ₁₆ | At reset | Non-maskable |
| INT ₀ | 2 | FFFB ₁₆ | FFFA ₁₆ | At detection of either rising or falling edge of INT ₀ input | External interrupt (active edge selectable) |
| INT ₁ | 3 | FFF9 ₁₆ | FFF8 ₁₆ | At detection of either rising or falling edge of INT ₁ input | External interrupt (active edge selectable) |
| Serial I/O1 reception | 4 | FFF7 ₁₆ | FFF6 ₁₆ | At completion of serial I/O1 data reception | Valid when serial I/O1 is selected |
| Serial I/O1 transmission | 5 | FFF5 ₁₆ | FFF4 ₁₆ | At completion of serial I/O1 transmit shift or when transmission buffer is empty | Valid when serial I/O1 is selected |
| Timer X | 6 | FFF3 ₁₆ | FFF2 ₁₆ | At timer X underflow | |
| Timer Y | 7 | FFF1 ₁₆ | FFF0 ₁₆ | At timer Y underflow | |
| Timer 2 | 8 | FFEF ₁₆ | FFEE ₁₆ | At timer 2 underflow | |
| Timer 3 | 9 | FFED ₁₆ | FFEC ₁₆ | At timer 3 underflow | |
| CNTR ₀ | 10 | FFEB ₁₆ | FFEA ₁₆ | At detection of either rising or falling edge of CNTR ₀ input | External interrupt (active edge selectable) |
| CNTR ₁ | 11 | FFE9 ₁₆ | FFE8 ₁₆ | At detection of either rising or falling edge of CNTR ₁ input | External interrupt (active edge selectable) |
| Timer 1 | 12 | FFE7 ₁₆ | FFE6 ₁₆ | At timer 1 underflow | |
| INT ₂ | 13 | FFE5 ₁₆ | FFE4 ₁₆ | At detection of either rising or falling edge of INT ₂ input | External interrupt (active edge selectable) |
| Serial I/O2 | 14 | FFE3 ₁₆ | FFE2 ₁₆ | At completion of serial I/O2 data transmission or reception | Valid when serial I/O2 is selected |
| Key input (Key-on wake-up) | 15 | FFE1 ₁₆ | FFE0 ₁₆ | At falling of conjunction of input level for port P2 (at input mode) | External interrupt (valid at falling) |
| ADT | 16 | FFDF ₁₆ | FFDE ₁₆ | At falling edge of ADT input | Valid when ADT interrupt is selected External interrupt (valid at falling) |
| A-D conversion | | | | At completion of A-D conversion | Valid when A-D interrupt is selected |
| BRK instruction | 17 | FFDD ₁₆ | FFDC ₁₆ | At BRK instruction execution | Non-maskable software interrupt |

Notes1: Vector addresses contain interrupt jump destination addresses.

2: Reset is not an interrupt. Reset has the higher priority than all interrupts.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to "1".

- When switching external interrupt active edge
 Related register: Interrupt edge selection register (address 3A16)
 Timer X mode register (address 2716)
 Timer Y mode register (address 2816)
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
 Related register: Interrupt source selection bit of A-D control register (bit 6 of address 3416)

When not requiring for the interrupt occurrence synchronous with these setting, take the following sequence.

- ①Set the corresponding interrupt enable bit to "0" (disabled).
- ②Set the interrupt edge select bit (polarity switch bit) or the interrupt source selection bit.
- ③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④Set the corresponding interrupt enable bit to "1" (enabled).

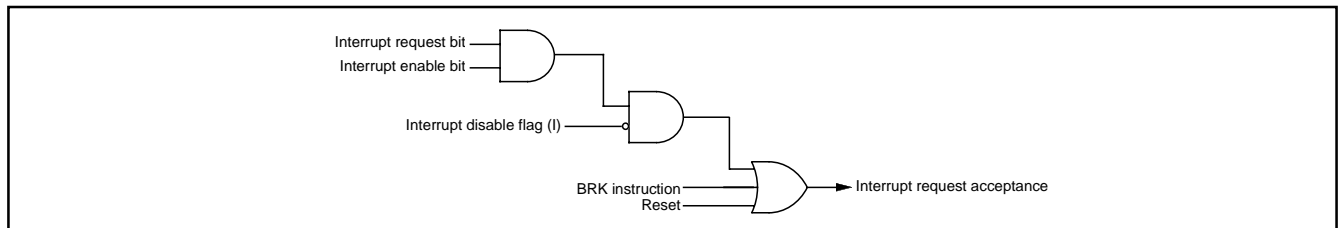


Fig. 20 Interrupt control

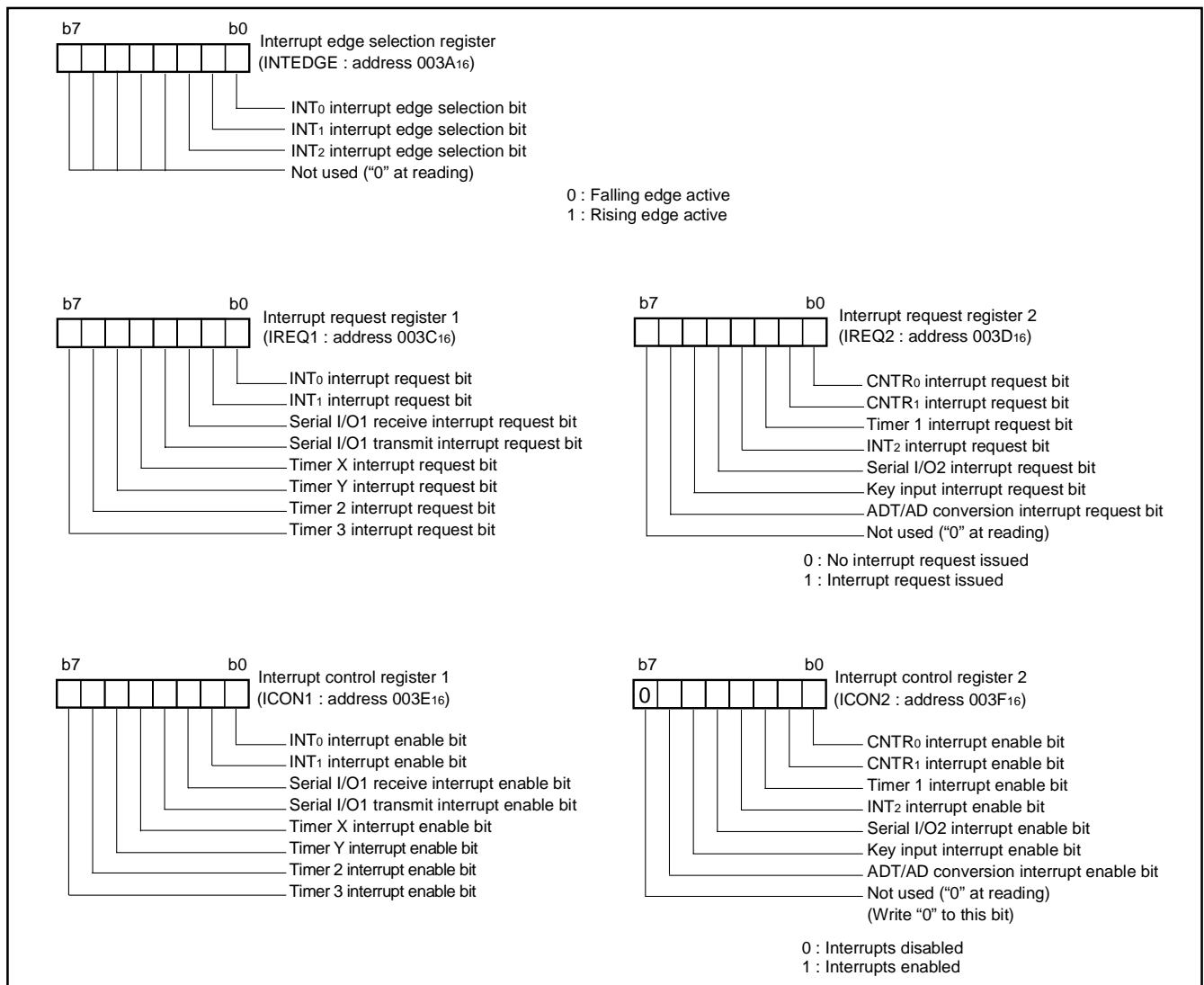


Fig. 21 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake Up)

The key input interrupt is enabled when any of port P2 is set to input mode and the bit corresponding to key input control register is set to "1".

A Key input interrupt request is generated by applying "L" level voltage to any pin of port P2 of which key input interrupt is en-

abled. In other words, it is generated when AND of input level goes from "1" to "0". A connection example of using a key input interrupt is shown in Figure 22, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P20–P23.

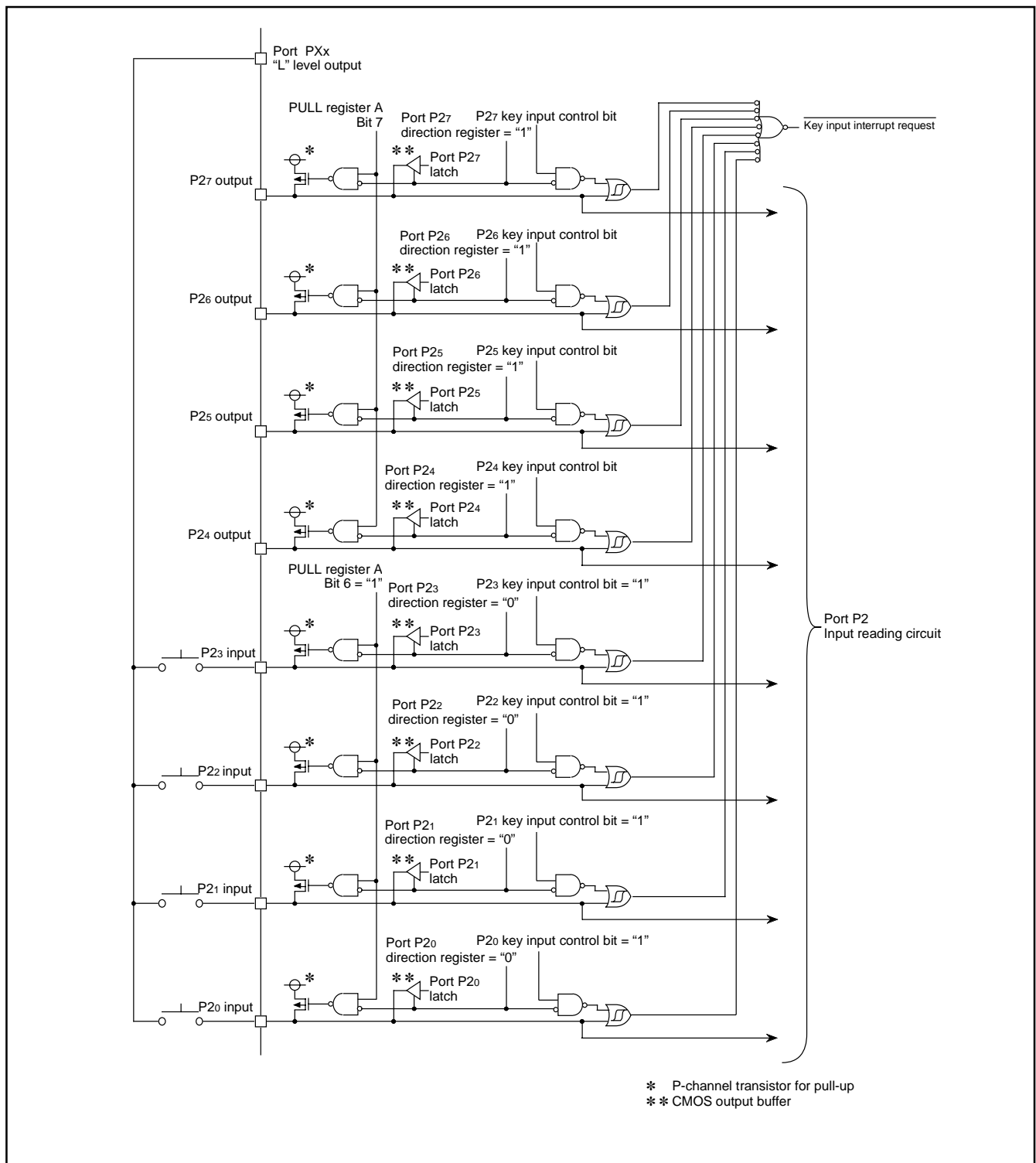


Fig. 22 Connection example when using key input interrupt and port P2 block diagram

The key input interrupt is controlled by the key input control register and the port direction register. When enabling the key input interrupt, set "1" to the key input control bit. A key input can be accepted from pins set as the input mode in ports P20–P27.

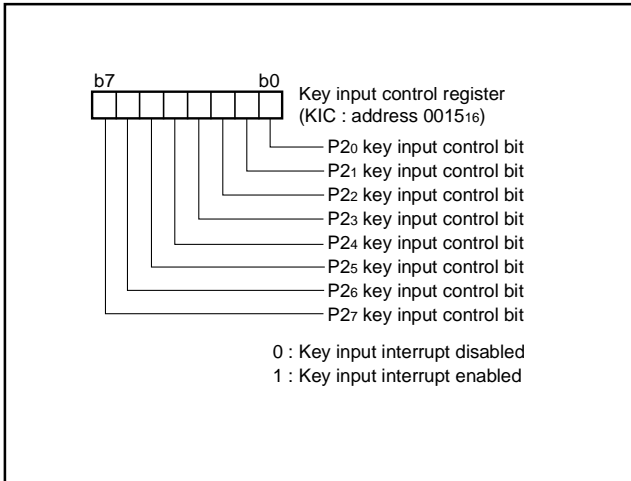


Fig. 23 Structure of key input control register

TIMERS

The 7560 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "0", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

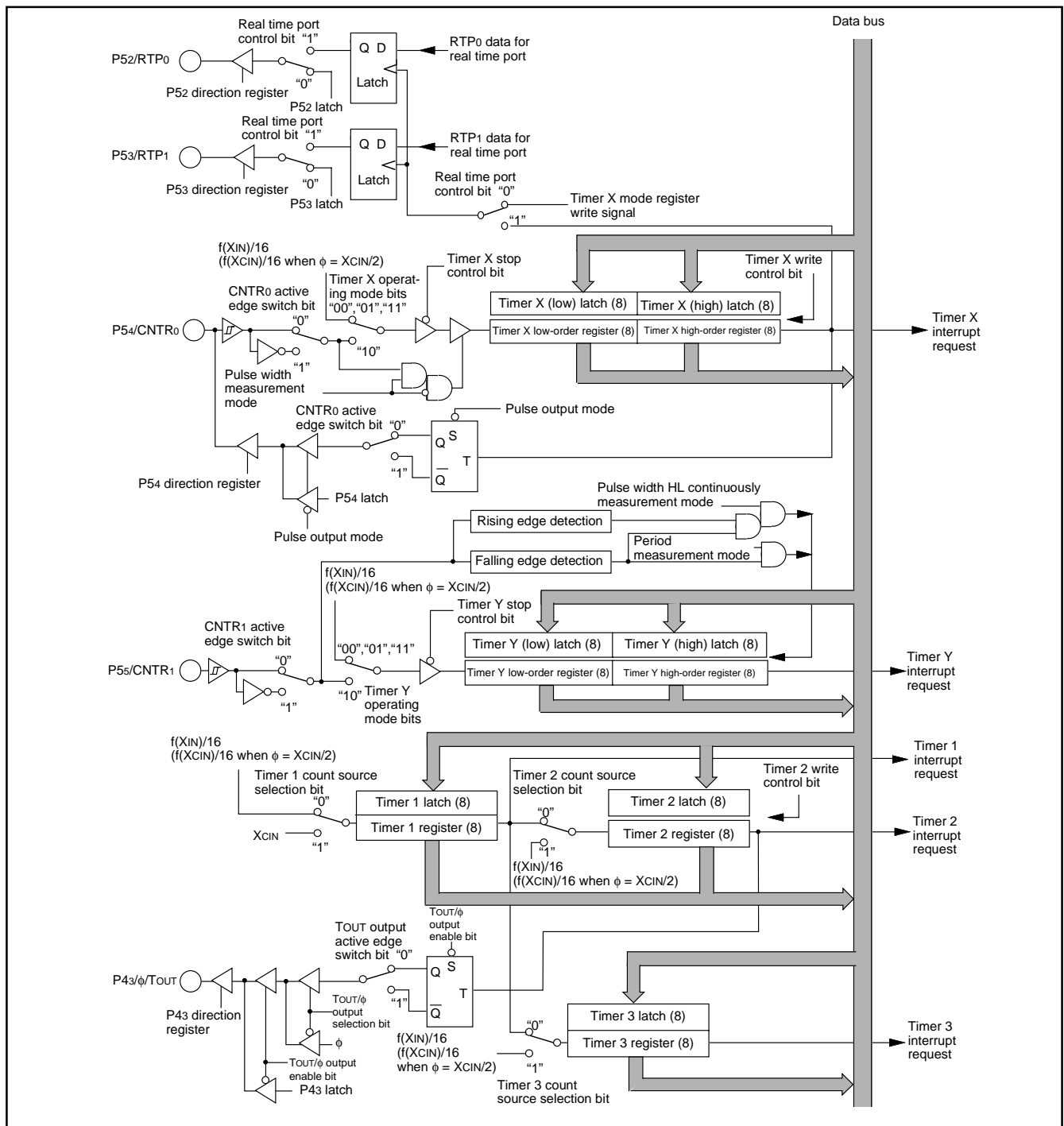


Fig. 24 Timer block diagram

Timer X

Timer X is a 16-bit timer and is equipped with the timer latch. The division ratio of timer X is given by $1/(n+1)$, where n is the value in the timer latch. Timer X is a down-counter. When the contents of timer X reach "0000₁₆", an underflow occurs at the next count pulse and the contents of the timer latch are reloaded into the timer and the count is continued. When the timer underflows, the timer X interrupt request bit is set to "1".

Timer X can be selected in one of four modes by the timer X mode register and can be controlled the timer X write and the real time port.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Pulse output mode

Each time the timer underflows, a signal output from the CNTR₀ pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the P5₄/CNTR₀ pin to output mode (set "1" to bit 4 of port P5 direction register).

(3) Event counter mode

The timer counts signals input through the CNTR₀ pin. Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the P5₄/CNTR₀ pin to input mode (set "0" to bit 4 of port P5 direction register).

(4) Pulse width measurement mode

The count source is $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode). If CNTR₀ active edge switch bit is "0", the timer counts while the input signal of CNTR₀ pin is at "H". If it is "1", the timer counts while the input signal of CNTR₀ pin is at "L". When using a timer in this mode, set the P5₄/CNTR₀ pin to input mode (set "0" to bit 4 of port P5 direction register).

●Read and write to timer X high-order, low-order registers

When reading and writing to the timer X high-order and low-order registers, be sure to read/write both the timer X high- and low-order registers.

When reading the timer X high-order and low-order registers, read the high-order register first. When writing to the timer X high-order and low-order registers, write the low-order register first. The timer X cannot perform the correct operation if the next operation is performed.

- Write operation to the high- or low-order register before reading the timer X low-order register
- Read operation from the high- or low-order register before writing to the timer X high-order register

●Timer X Write Control

Which write control can be selected by the timer X write control bit (bit 0) of the timer X mode register (address 0027₁₆), writing data to both the latch and the timer at the same time or writing data only to the latch. When the operation "writing data only to the latch" is selected, the value is set to the timer latch by writing data to the timer X register and the timer is updated at next underflow. After reset, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the latch and the timer at the same time by writing data to the timer X register. The write operation is independent of timer X count operation, operating or stopping.

When the value is written in latch only, a value is simultaneously set to the timer X and the timer X latch if the writing in the high-order register and the underflow of timer X are performed at the same timing. Unexpected value may be set in the high-order timer on this occasion.

●Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports P5₂ and P5₃ each time the timer X underflows. (However, if the real time port control bit is changed from "0" to "1" after set of the real time port data, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.

Before using this function, set the P5₂/RTP₀, P5₃/RTP₁ pins to output mode (set "1" to bits 2, 3 of port P5 direction register).

■Note on CNTR₀ interrupt active edge selection

CNTR₀ interrupt active edge depends on the CNTR₀ active edge switch bit.

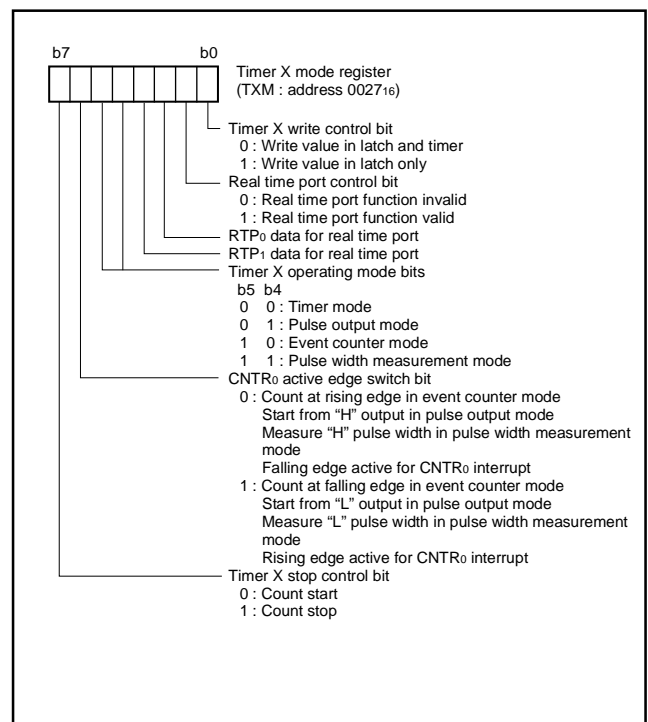


Fig. 25 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer and is equipped with the timer latch. The division ratio of timer Y is given by $1/(n+1)$, where n is the value in the timer latch. Timer Y is a down-counter. When the contents of timer Y reach "0000₁₆", an underflow occurs at the next count pulse and the contents of the timer latch are reloaded into the timer and the count is continued. When the timer underflows, the timer Y interrupt request bit is set to "1".

Timer Y can be selected in one of four modes by the timer Y mode register.

(1) Timer mode

The timer counts $f(XIN)/16$ (or $f(XCIN)/16$ in low-speed mode).

(2) Period measurement mode

CNTR1 interrupt request is generated at rising or falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for this, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising or falling of CNTR1 pin input signal is retained until the next valid edge is input.

The rising or falling timing of CNTR1 pin input signal can be discriminated by CNTR1 interrupt. When using a timer in this mode, set the P55/CNTR1 pin to input mode (set "0" to bit 5 of port P5 direction register).

(3) Event counter mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the P55/CNTR1 pin to input mode (set "0" to bit 5 of port P5 direction register).

(4) Pulse width HL continuously measurement mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the P55/CNTR1 pin to input mode (set "0" to bit 5 of port P5 direction register).

■Note on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the value of the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the value of CNTR1 active edge switch bit.

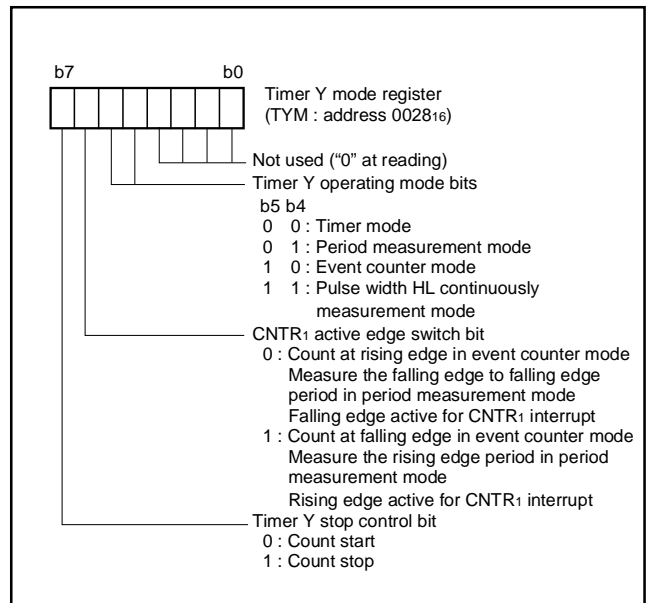


Fig. 26 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers and is equipped with the timer latch. The count source for each timer can be selected by the timer 123 mode register.

The division ratio of each timer is given by $1/(n+1)$, where n is the value in the timer latch. All timers are down-counters. When the contents of the timer reach "00₁₆", an underflow occurs at the next count pulse and the contents of the timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

When a value is written to the timer 1 register and the timer 3 register, a value is simultaneously set as the timer latch and the timer. When the timer 1 register, the timer 2 register, or the timer 3 register is read, the count value of the timer can be read.

●Timer 2 Write Control

Which write can be selected by the timer 2 write control bit (bit 2) of the timer 123 mode register (address 0029₁₆), writing data to both the latch and the timer at the same time or writing data only to the latch. When the operation "writing data only to the latch" is selected, the value is set to the timer 2 latch by writing data to the timer 2 register and the timer 2 is updated at next underflow. After reset, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the timer 2 latch and the timer 2 at the same time by writing data to the timer 2 register.

If the value is written in latch only, a value is simultaneously set to the timer 2 and the timer 2 latch when the writing in the high-order register and the underflow of timer 2 are performed at the same timing.

●Timer 2 Output Control

When the timer 2 (TOUT) output is enabled by the TOUT/ ϕ output enable bit and the TOUT/ ϕ output selection bit, an inversion signal from the TOUT pin is output each time timer 2 underflows.

In this case, set the P43/ ϕ /TOUT pin to output mode (set "1" to bit 3 of port P4 direction register).

■Note on Timer 1 to Timer 3

When the count source of timers 1 to 3 is changed, the timer counting value may become arbitrary value because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may become undefined value because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

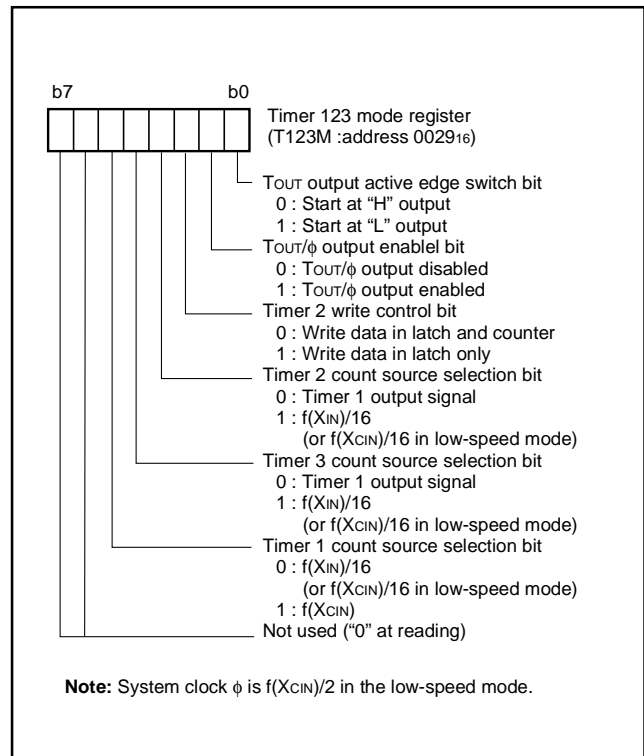


Fig. 27 Structure of timer 123 mode register

SERIAL I/O
Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode is selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register to "1". For clock synchronous serial I/O mode, the transmitter and the receiver must use the same clock as an operation clock.

When an internal clock is selected as an operation clock, transmit or receive is started by a write signal to the transmit buffer register.

When an external clock is selected as an operation clock, serial I/O1 becomes the state where transmit or receive can be performed by a write signal to the transmit buffer register. Transmit and receive are started by input of an external clock.

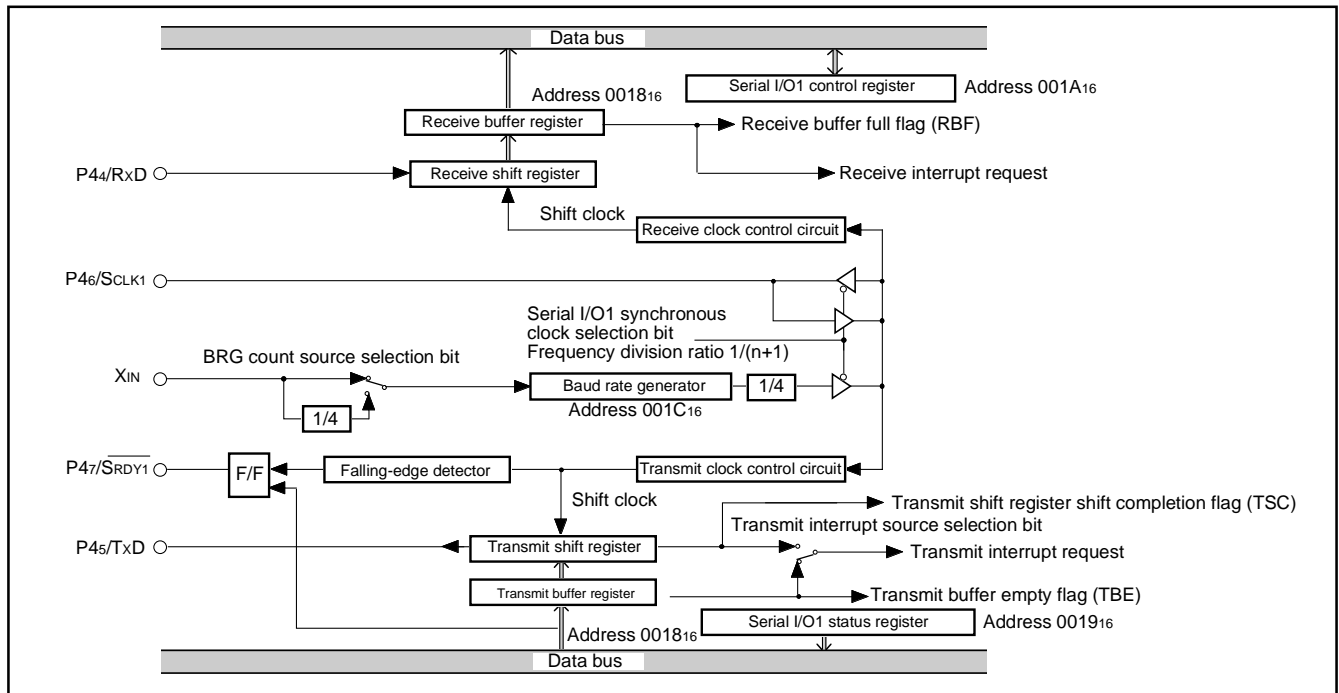


Fig. 28 Block diagram of clock synchronous serial I/O1

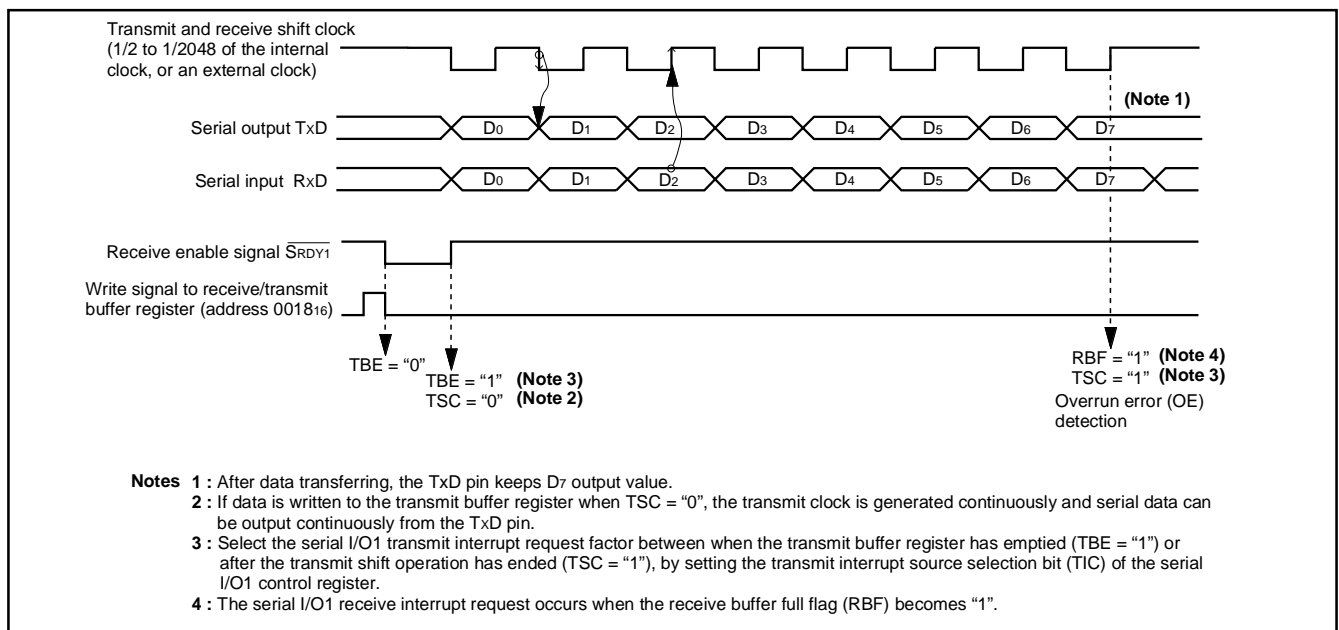


Fig. 29 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) is selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer regis-

ter, but the two buffers have the same address (0018₁₆) in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted during transmitting, and the receive buffer register can hold received one-byte data while the next one-byte data is being received.

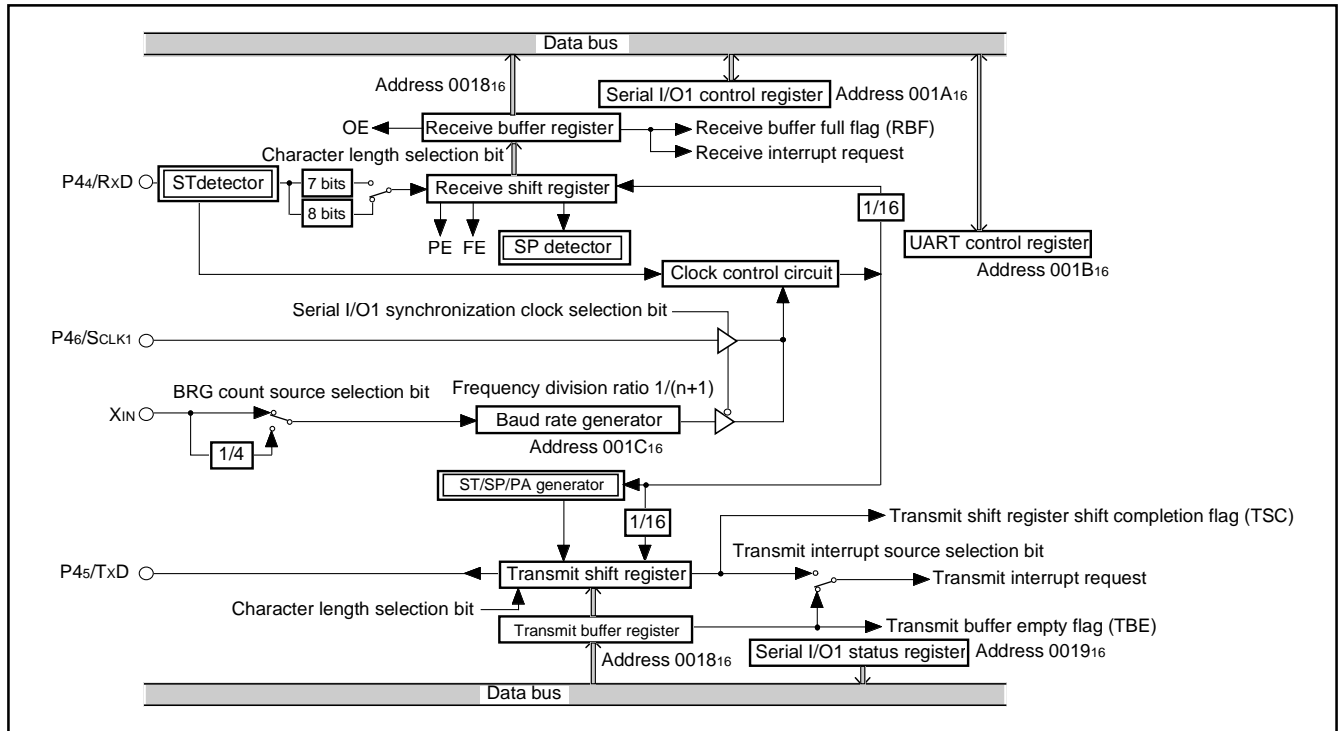


Fig. 30 Block diagram of UART serial I/O1

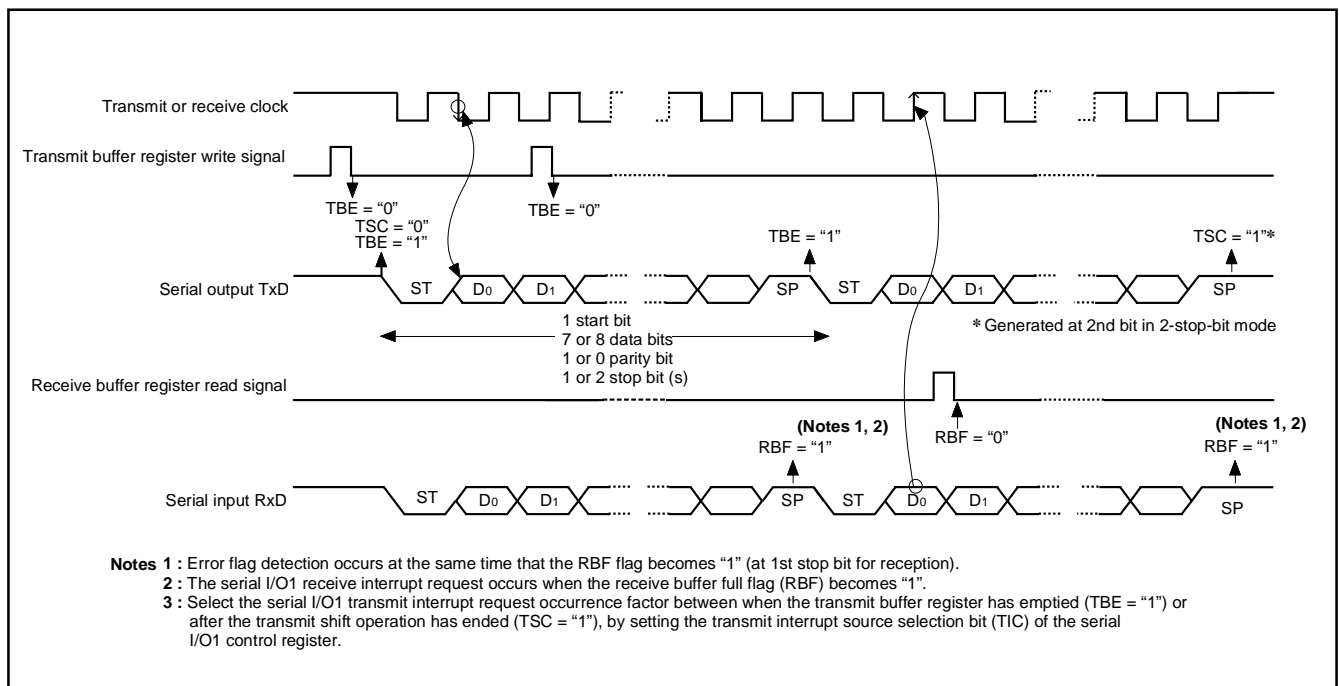


Fig. 31 Operation of UART serial I/O1 function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018₁₆

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is "0".

[Serial I/O1 Status Register (SIO1STS)] 0019₁₆

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is set to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set to "1". A write signal to the serial I/O1 status register sets all the error flags (OE, PE, FE, and SE) (bit 3 to bit 6, respectively) to "0". Writing "0" to the serial I/O1 enable bit (SIOE) also sets all the status flags to "0", including the error flags.

All bits of the serial I/O1 status register are set to "0" at reset, but if the transmit enable bit of the serial I/O1 control register has been set to "1", the transmit shift register shift completion flag and the transmit buffer empty flag become "1".

[Serial I/O1 Control Register (SIO1CON)] 001A₁₆

The serial I/O1 control register contains eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] 001B₁₆

The UART control register consists of the bits which set the data format of an data transmit and receive, and the bit which sets the output structure of the P45/TxD pin.

[Baud Rate Generator (BRG)] 001C₁₆

The baud rate generator is the 8-bit counter equipped with a reload register. Set the division value of the BRG count source to the baud rate generator.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to "1", the serial I/O1 transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronous with the transmission enabled, take the following sequence.

- ①Set the serial I/O1 transmit interrupt enable bit to "0" (disabled).
- ②Set the transmit enable bit to "1".
- ③Set the serial I/O1 transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ④Set the serial I/O1 transmit interrupt enable bit to "1" (enabled).

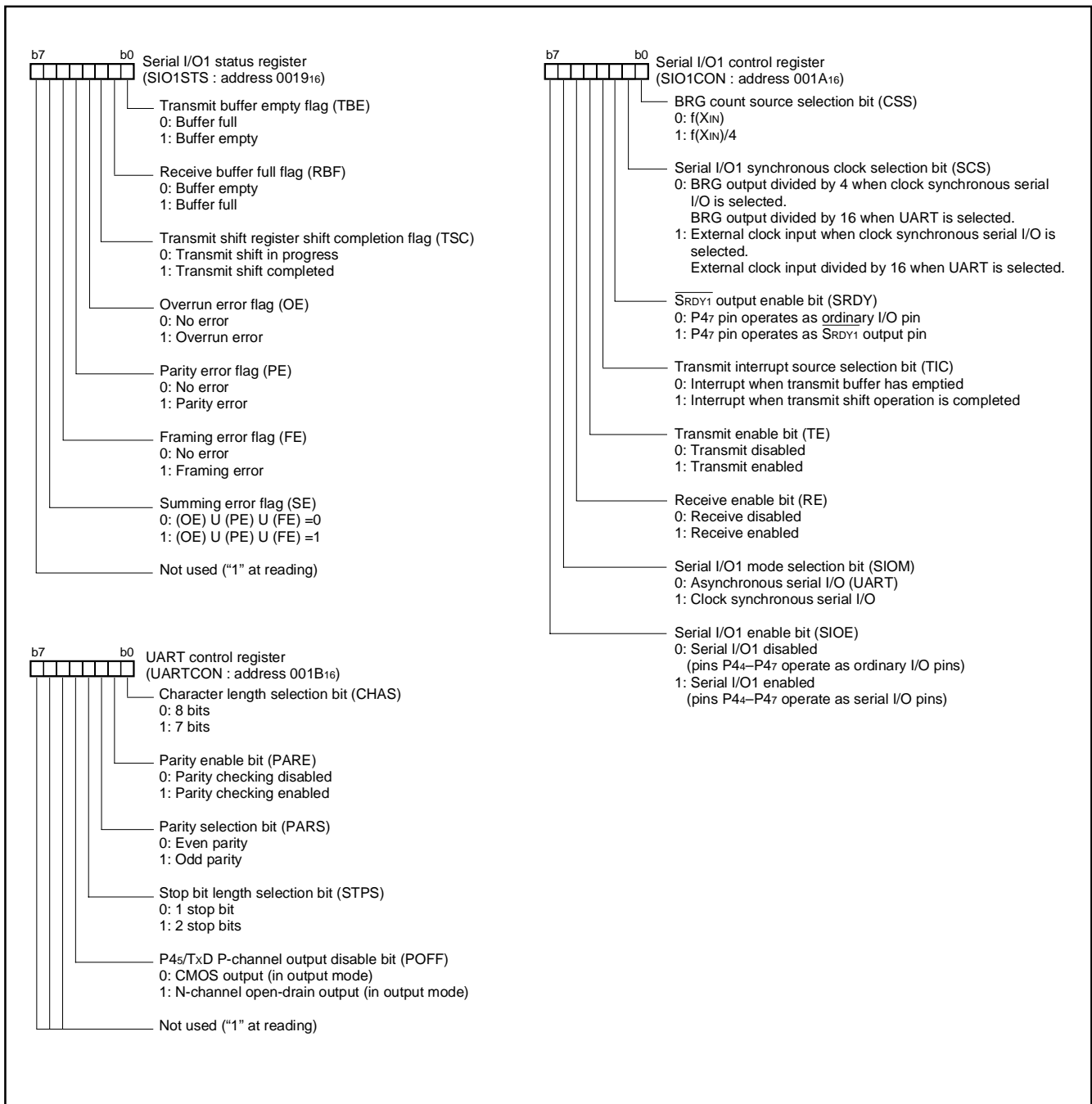


Fig. 32 Structure of serial I/O1 control registers

Serial I/O2

Serial I/O2 can be used only for clock synchronous serial I/O. For serial I/O2, the transmitter and the receiver must use the same clock as a synchronous clock. When an internal clock is selected as a synchronous clock, the serial I/O2 is initialized and, transmit and receive is started by a write signal to the serial I/O2 register.

When an external clock is selected as a synchronous clock, the serial I/O2 counter is initialized by a write signal to the serial I/O2 register, serial I/O2 becomes the state where transmission or reception can be performed. Write to the serial I/O2 register while SCLK21 is "H" state when an external clock is selected as a synchronous clock.

Either P62/SCLK21 or P63/SCLK22 pin can be selected as an output pin of the synchronous clock. In this case, the pin that is not selected as an output pin of the synchronous clock functions as a I/O port.

[Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains eight control bits for the serial I/O2 functions. After setting to this register, write data to the serial I/O2 register and start transmit and receive.

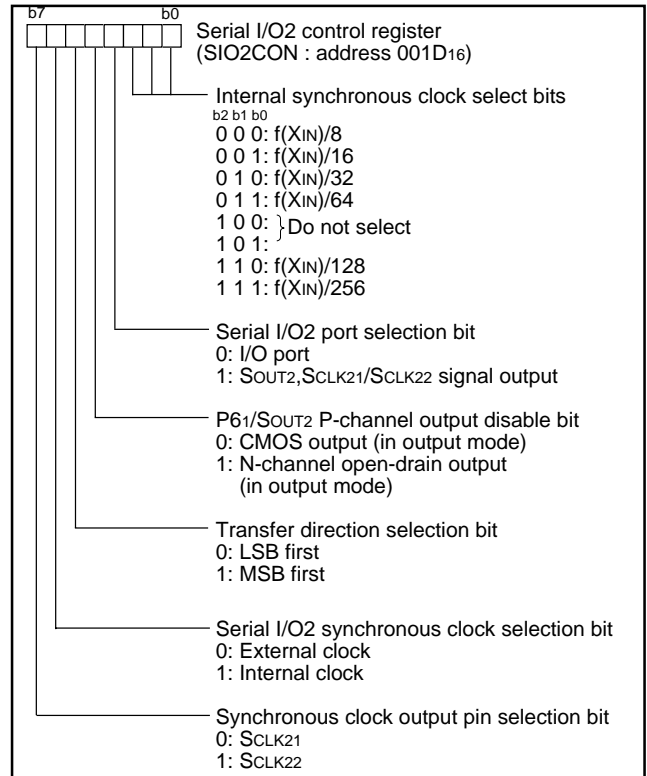


Fig. 33 Structure of serial I/O2 control register

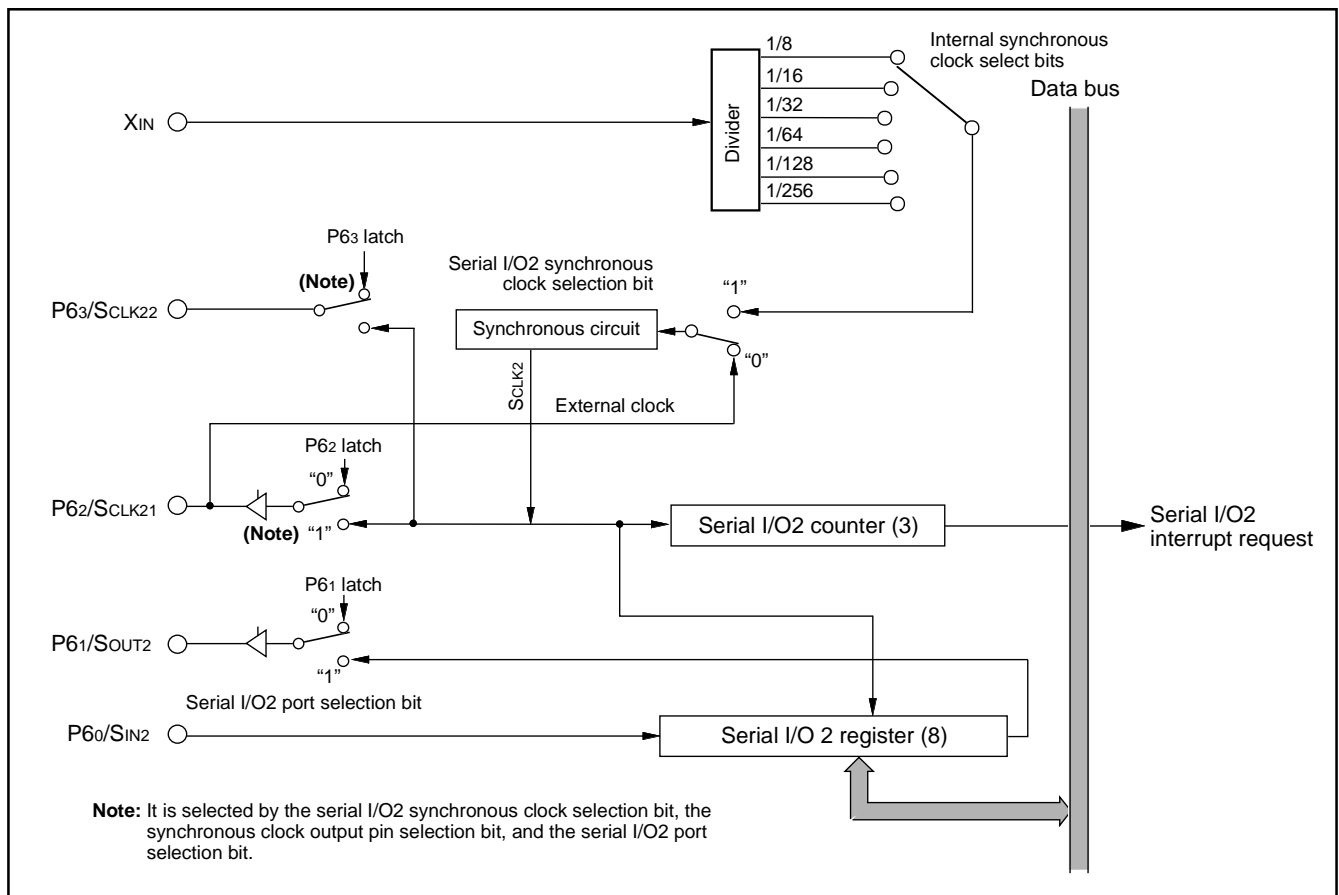


Fig. 34 Block diagram of serial I/O2 function

●Serial I/O2 Operating

The serial I/O2 counter is initialized to "7" by writing to the serial I/O2 register.

After writing, whenever a synchronous clock changes from "H" to "L", data is output from the SOUT2 pin. Moreover, whenever a synchronous clock changes from "L" to "H", data is taken in from the SIN2 pin, and 1 bit shift of the serial I/O2 register is carried out simultaneously.

When the internal clock is selected as a synchronous clock, it is as follows if a synchronous clock is counted 8 times.

- Serial I/O2 counter = "0"
- Synchronous clock stops in "H" state
- Serial I/O2 interrupt request bit = "1"

The SOUT2 pin is in a high impedance state after transfer is completed.

When the external clock is selected as a synchronous clock, if a synchronous clock is counted 8 times, the serial I/O2 interrupt request bit is set to "1", and the SOUT2 pin holds the output level of D7. However, if a synchronous clock continues being input, the shift of the serial I/O2 register is continued and transmission data continues being output from the SOUT2 pin.

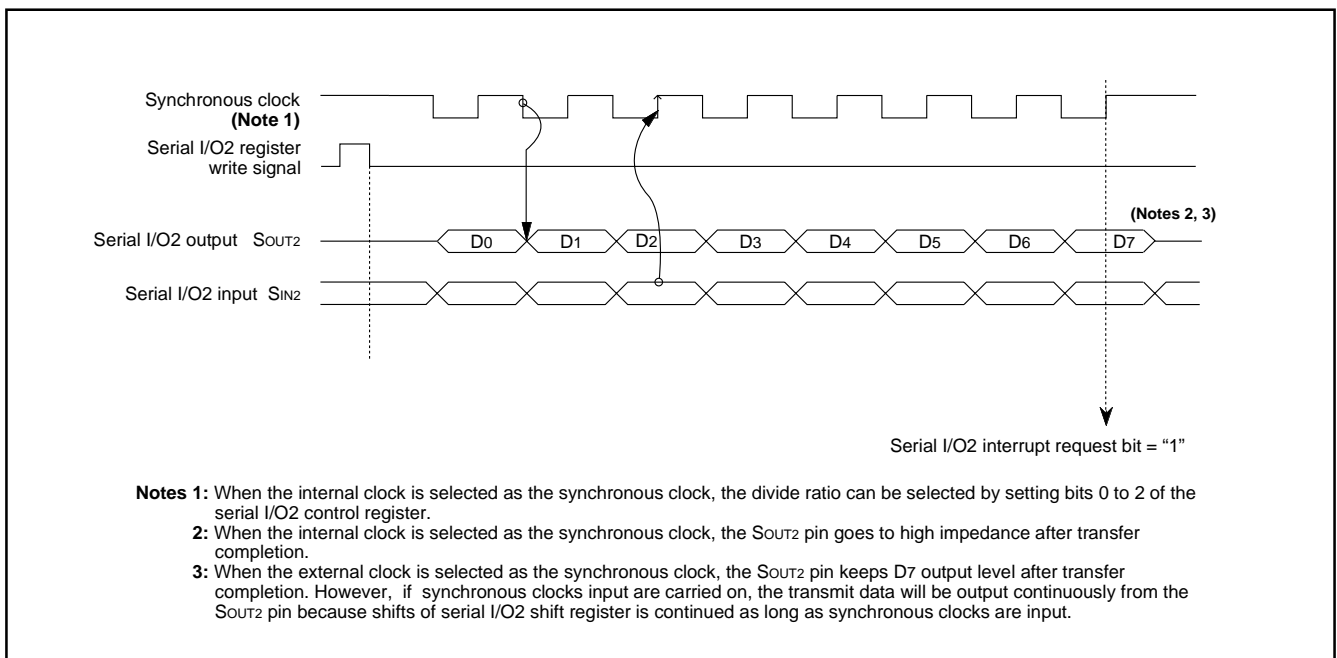


Fig. 35 Timing of serial I/O2 function

PULSE WIDTH MODULATION (PWM)

The 7560 group has a PWM function with an 8-bit resolution, using $f(X_{IN})$ or $f(X_{IN})/2$ as a count source.

Data Setting

The PWM output pins are shared with ports P50 and P51. Set the PWM period by the PWM prescaler, and set the period during which the output pulse is an "H" by the PWM register.

If PWM count source is $f(X_{IN})$ and the value in the PWM prescaler is n and the value in the PWM register is m (where $n = 0$ to 255 and $m = 0$ to 255) :

$$\begin{aligned} \text{PWM period} &= 255 \times (n+1)/f(X_{IN}) \\ &= 31.875 \times (n+1) \mu\text{s} \text{ (when } f(X_{IN}) = 8 \text{ MHz)} \end{aligned}$$

$$\begin{aligned} \text{Output pulse "H" period} &= \text{PWM period} \times m/255 \\ &= 0.125 \times (n+1) \times m \mu\text{s} \\ &\text{(when } f(X_{IN}) = 8 \text{ MHz)} \end{aligned}$$

PWM Operation

When either bit 1 (PWM0 function enable bit) or bit 2 (PWM1 function enable bit) of the PWM control register or both bits are enabled, operation starts from initializing status, and pulses are output starting at "H". When one PWM output is enabled and that the other PWM output is enabled, PWM output which is enabled to output later starts pulse output from halfway of PWM period (see Figure 39).

When the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

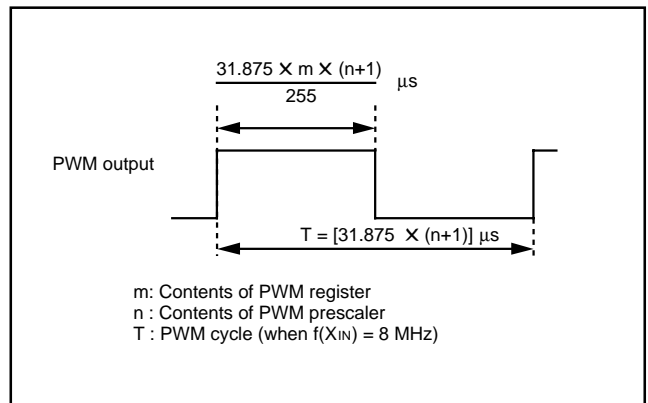


Fig. 36 Timing of PWM cycle

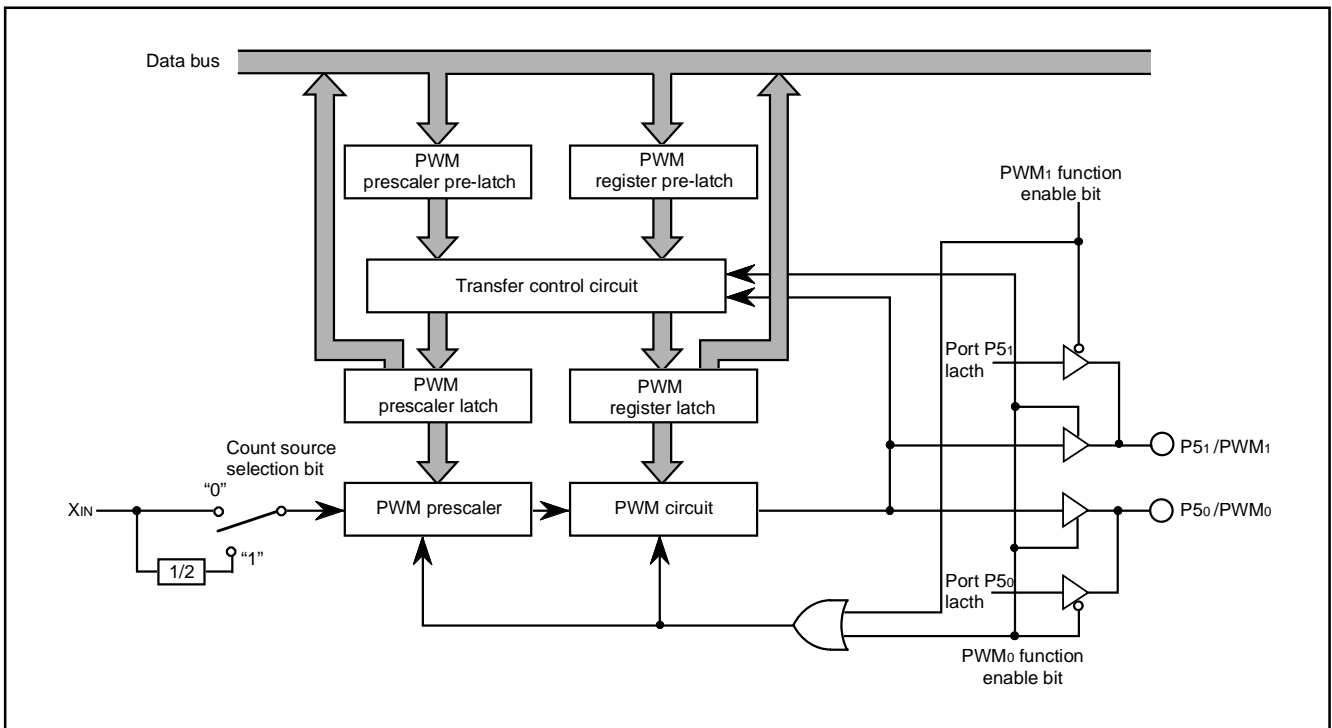


Fig. 37 Block diagram of PWM function

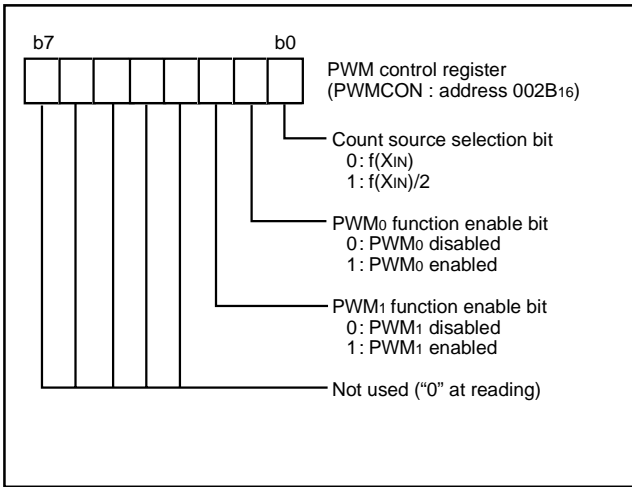


Fig. 38 Structure of PWM control register

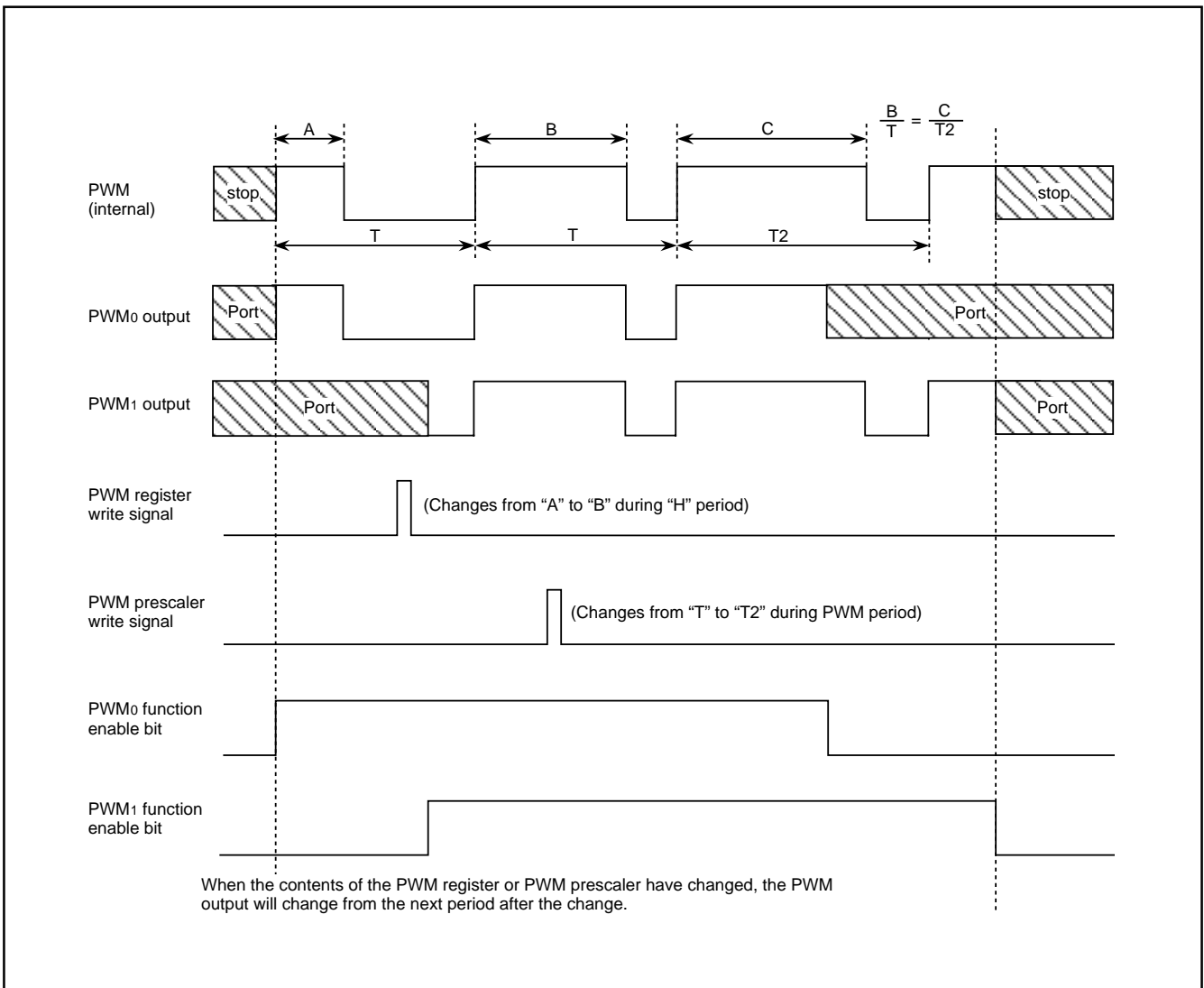


Fig. 39 PWM output timing when PWM register or PWM prescaler is changed

A-D CONVERTER

[A-D Conversion Low-Order Register (ADL)] 001416

[A-D Conversion High-Order Register (ADH)] 003516

The A-D conversion registers are read-only registers that store the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

The high-order 8 bits of a conversion result is stored in the A-D conversion high-order register (address 003516), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A-D conversion low-order register (address 001416).

Bit 0 of the A-D conversion low-order register is the conversion mode selection bit. When this bit is set to "0", that becomes the 10-bit A-D mode. When this bit is set to "1", that becomes the 8-bit A-D mode.

[A-D Control Register (ADCON)] 003416

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 indicates the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then it is set to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion.

Bit 4 is the VREF input switch bit which controls connection of the resistor ladder and the reference voltage input pin (VREF). The resistor ladder is always connected to VREF when bit 4 is set to "1". When bit 4 is set to "0", the resistor ladder is cut off from VREF except for A-D conversion performed. When bit 5, which is the AD external trigger valid bit, is set to "1", A-D conversion starts also by a falling edge of an ADT input. When using an A-D external trigger, set the P57/ADT pin to input mode (set "0" to bit 7 of port P5 direction register).

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF by 256 (when 8-bit A-D mode) or 1024 (when 10-bit A-D mode), and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports P67/AN7–P60/AN0.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD converter interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A-D conversion. Use the clock divided from the main clock f(XIN) as the system clock φ.

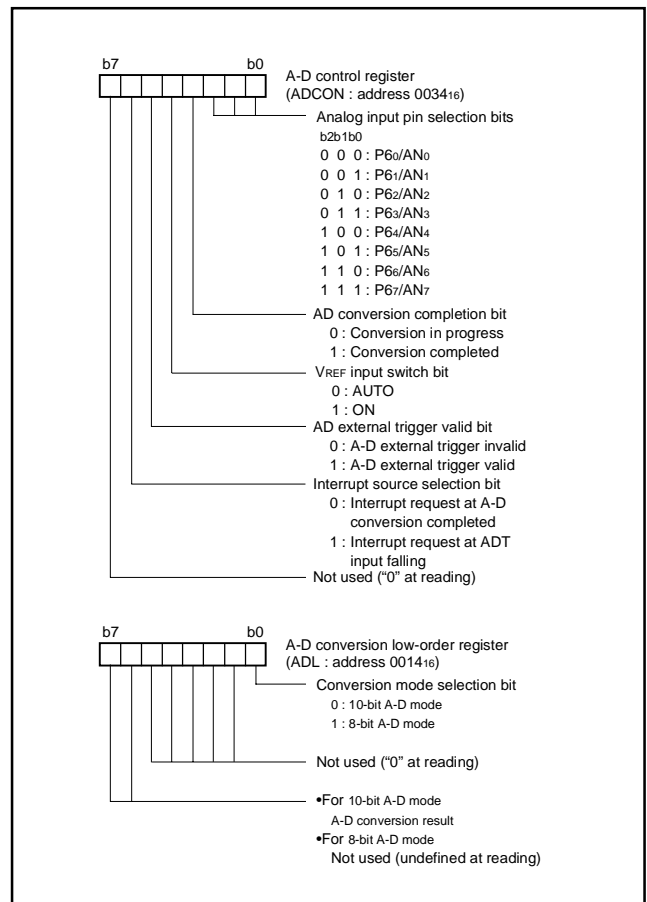


Fig. 40 Structure of A-D converter-related registers

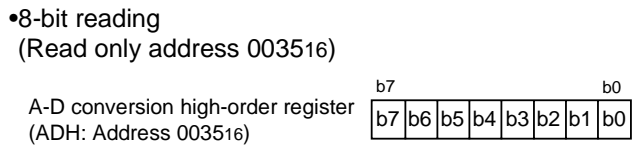
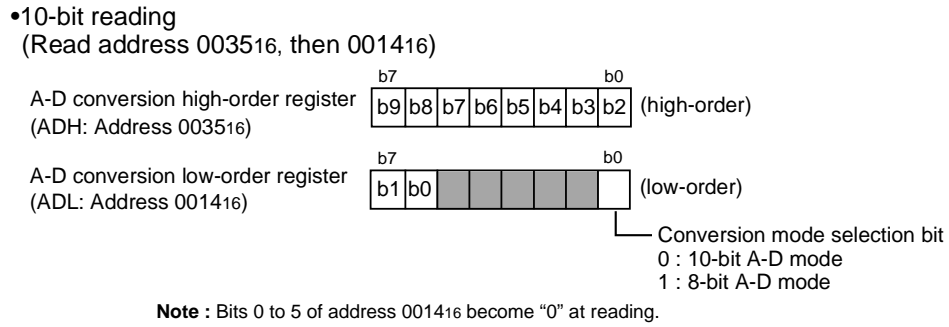


Fig. 41 Read of A-D conversion register

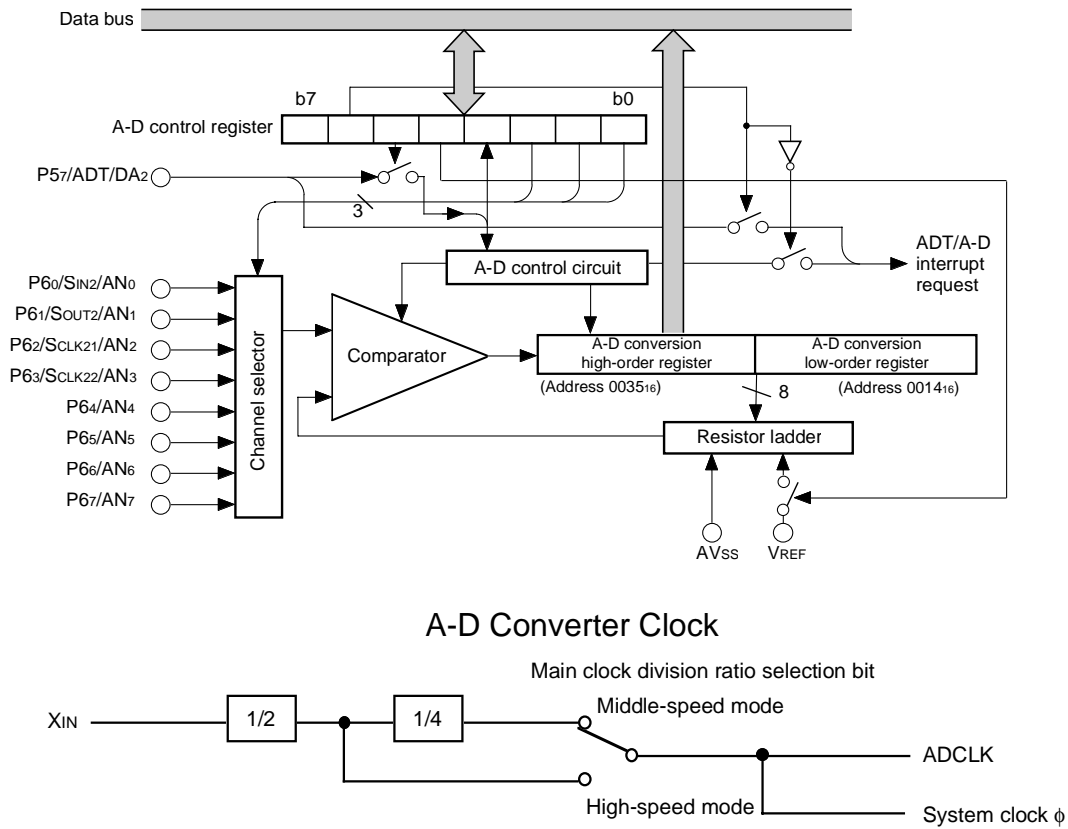


Fig. 42 A-D converter block diagram

D-A Converter

The 7560 group has a D-A converter with 8-bit resolution and 2 channels (DA1, DA2).

The D-A converter is started by setting the value in the D-A conversion register. When the DA1 output enable bit or the DA2 output enable bit is set to "1", the result of D-A conversion is output from the corresponding DA pin. When using the D-A converter, set the P56/DA1 pin and the P57/DA2 pin to input mode (set "0" to bits 6, 7 of port P5 direction register) and the pull-up resistor should be in the OFF state (set "0" to bit 3 of PULL register B) previously.

The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n=0 \text{ to } 255)$$

Where VREF is the reference voltage.

At reset, the D-A conversion registers are set to "0016", the DA1 output enable bit and the DA2 output enable bit are set to "0", and the P56/DA1 pin and the P57/DA2 pin goes to high impedance state. The DA converter is not buffered, so connect an external buffer when driving a low-impedance load.

■ **Note on applied voltage to VREF pin**

When these pins are used as D-A conversion output pins, the Vcc level is recommended for the applied voltage to VREF pin.

When the voltage below Vcc level is applied, the D-A conversion accuracy may be worse.

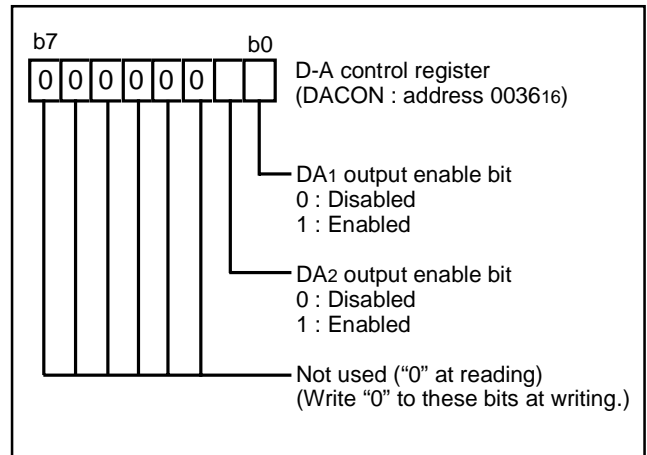


Fig. 43 Structure of D-A control register

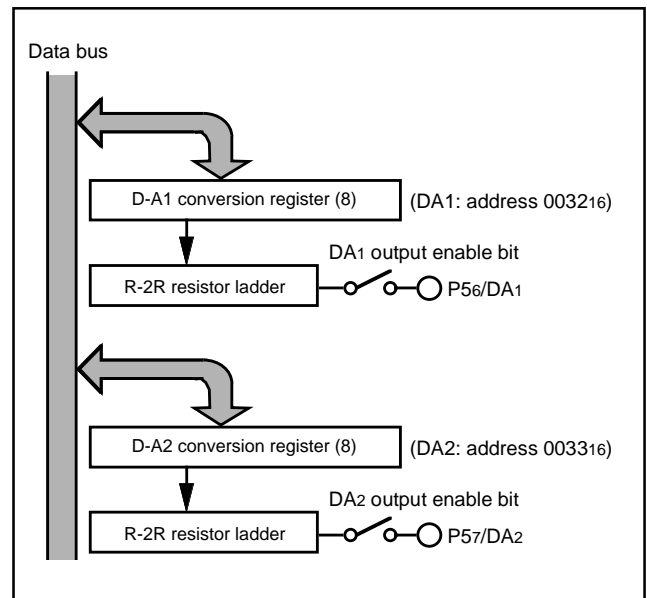


Fig. 44 Block diagram of D-A converter

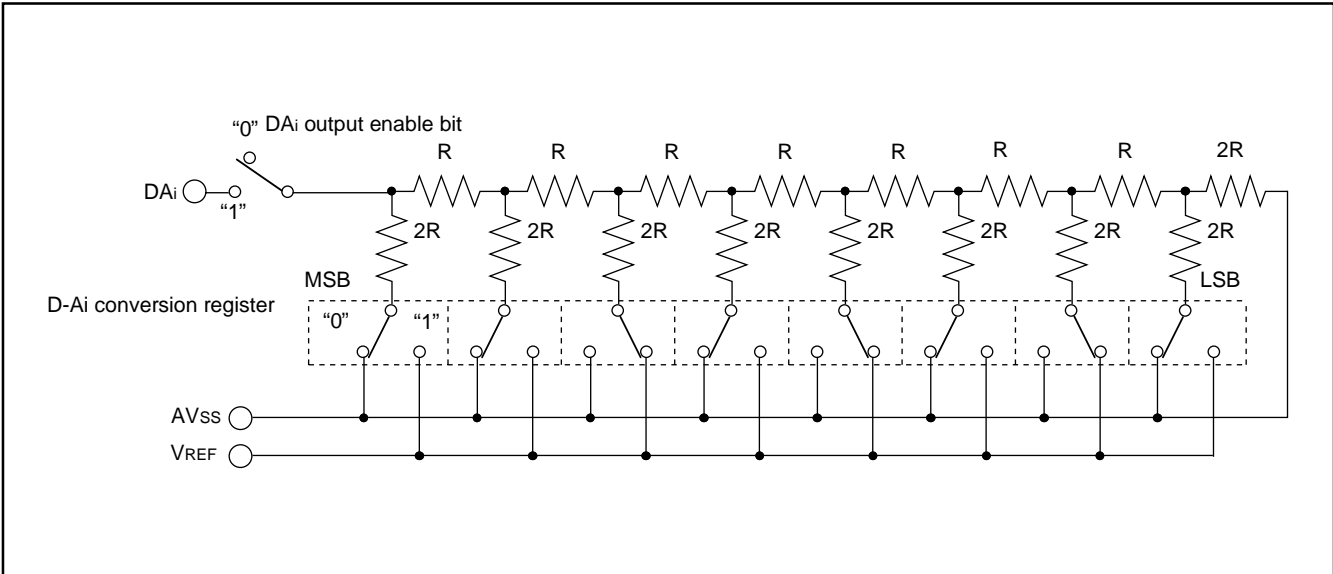


Fig. 45 Equivalent connection circuit of D-A converter

LCD DRIVE CONTROL CIRCUIT

The 7560 group has the Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output enable register
- LCD mode register
- Voltage multiplier
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 40 segment output pins and 4 common output pins can be used.

Up to 160 pixels can be controlled for LCD display. When the LCD

enable bit is set to "1" (LCD ON) after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 11 Maximum number of display pixels at each duty ratio

| Duty ratio | Maximum number of display pixel |
|------------|--|
| 2 | 80 dots or 8 segment LCD 10 digits |
| 3 | 120 dots or 8 segment LCD 15 digits |
| 4 | 160 dots or 8 segment LCD 20 digits |

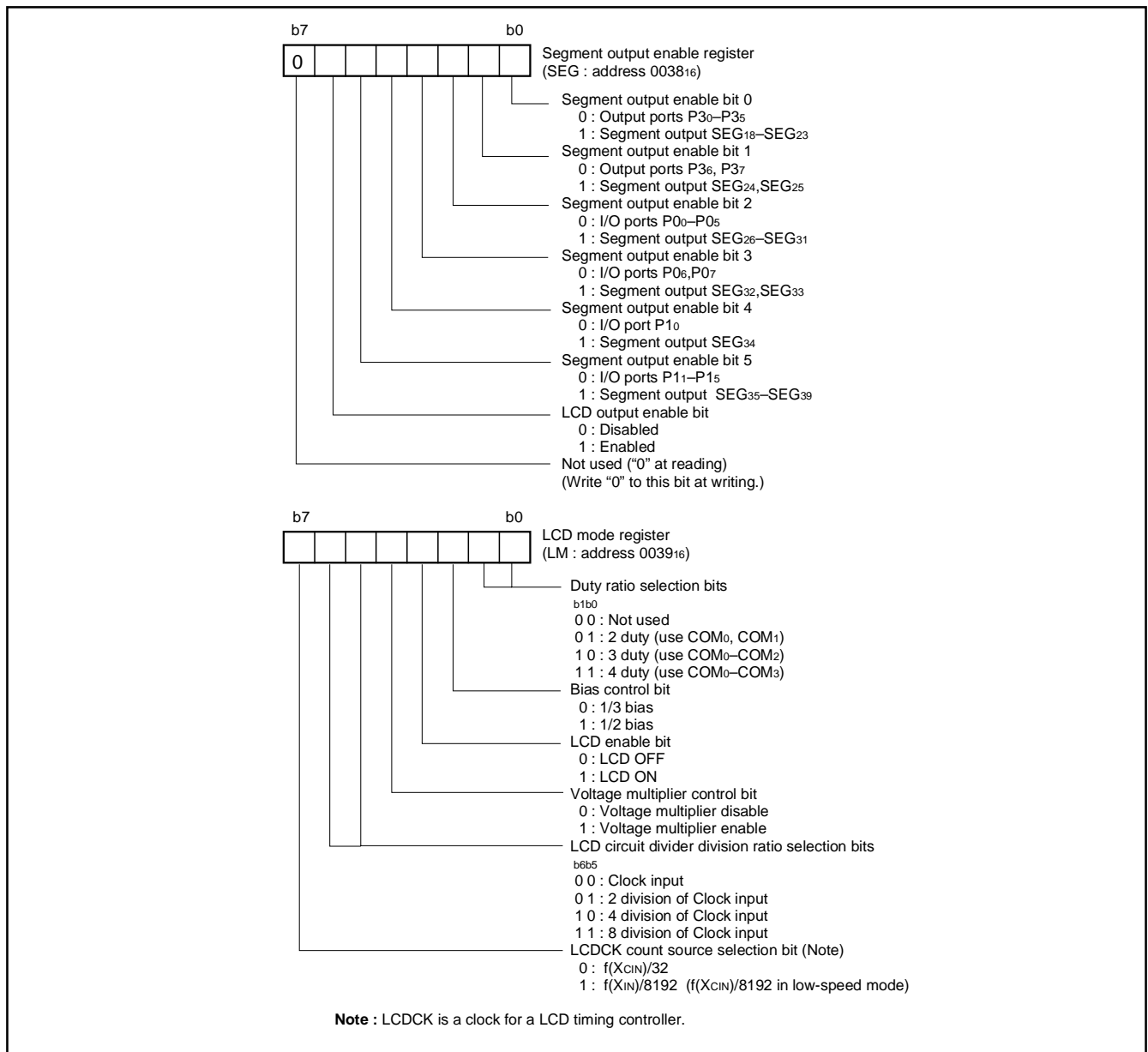


Fig. 46 Structure of segment output enable register and LCD mode register

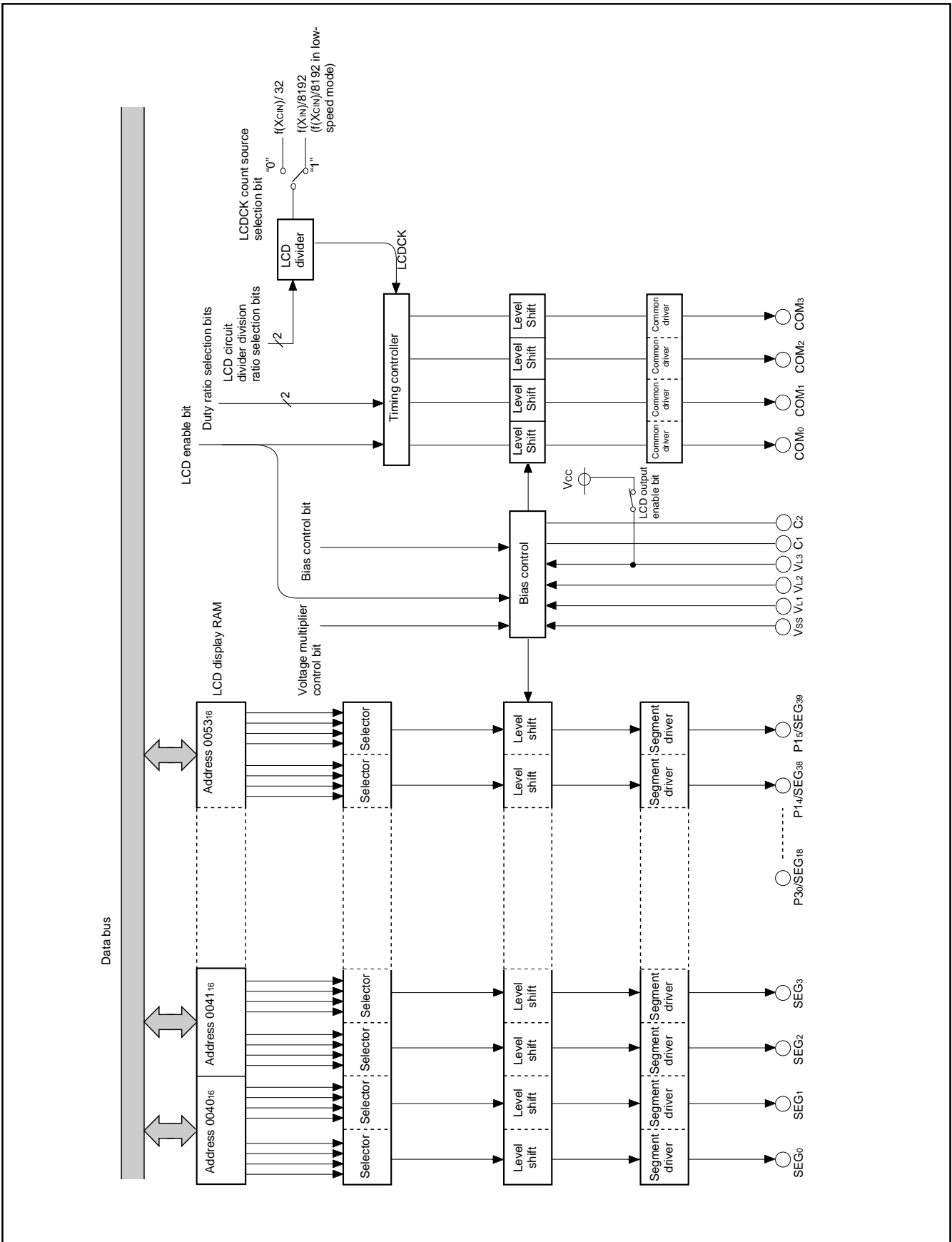


Fig. 47 Block diagram of LCD controller/driver

Voltage Multiplier (3 Times)

The voltage multiplier performs threefold boosting. This circuit inputs a reference voltage for boosting from LCD power input pin VL1.

Set each bit of the segment output enable register and the LCD mode register in the following order for operating the voltage multiplier.

1. Set the segment output enable bits (bits 0 to 5) of the segment output enable register to "0" or "1".
2. Set the duty ratio selection bits (bits 0 and 1), the bias control bit (bit 2), the LCD circuit divider division ratio selection bits (bits 5 and 6), and the LCDCK count source selection bit (bit 7) of the LCD mode register to "0" or "1".
3. Set the LCD output enable bit (bit 6) of the segment output enable register to "1". Apply the limit voltage or less to the VL1 pin.
4. Set the voltage multiplier control bit (bit 4) of the LCD mode register to "1". However, be sure to select 1/3 bias for bias control.

When voltage is input to the VL1 pin during operating the voltage multiplier, voltage that is twice as large as VL1 occurs at the VL2 pin, and voltage that is three times as large as VL1 occurs at the VL3 pin.

■Notes on Voltage Multiplier

When using the voltage multiplier, apply the limit voltage or less to the VL1 pin, then set the voltage multiplier control bit to "1" (enabled).

When not using the voltage multiplier, set the LCD output enable bit to "1", then apply proper voltage to the LCD power input pins (VL1-VL3).

When the LCD output enable bit is set to "0" (disabled), the VCC voltage is applied to the VL3 pin inside of this microcomputer.

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (VL1-VL3), apply the voltage shown in Table 12 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Table 12 Bias control and applied voltage to VL1-VL3

| Bias value | Voltage value |
|------------|--|
| 1/3 bias | VL3=VLCD VL2=2/3 VLCD VL1=1/3 VLCD |
| 1/2 bias | VL3=VLCD VL2=VL1=1/2 VLCD |

Note : VLCD is the maximum value of supplied voltage for the LCD panel.

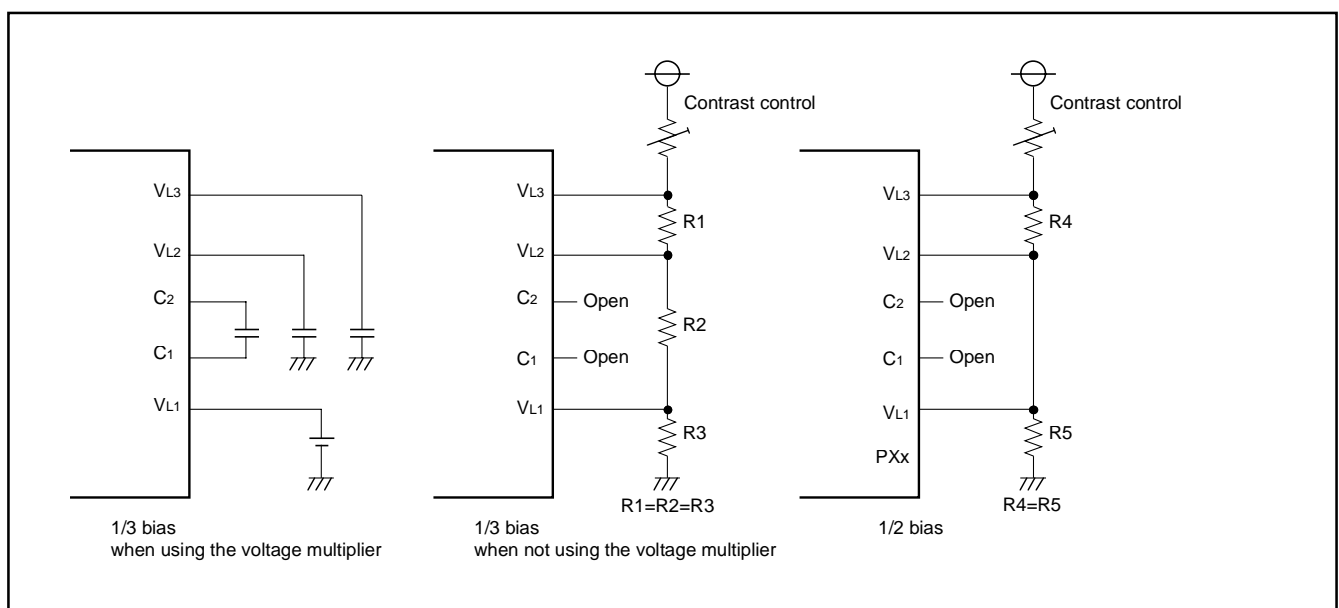


Fig. 48 Example of circuit at each bias

Common Pin and Duty Ratio Control

The common pins (COM0–COM3) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

After reset, the VCC (VL3) voltage is output from the common pins.

Table 13 Duty ratio control and common pins used

| Duty ratio | Duty ratio selection bits | | Common pins used |
|------------|---------------------------|-------|---------------------|
| | Bit 1 | Bit 0 | |
| 2 | 0 | 1 | COM0, COM1 (Note 1) |
| 3 | 1 | 0 | COM0–COM2 (Note 2) |
| 4 | 1 | 1 | COM0–COM3 |

Notes 1: COM2 and COM3 are open.
2: COM3 is open.

Segment Signal Output Pins

Segment signal output pins are classified into the segment-only pins (SEG0–SEG17), the segment or output port pins (SEG18–SEG25), and the segment or I/O port pins (SEG26–SEG39).

Segment signals are output according to the bit data of the LCD RAM corresponding to the duty ratio. After reset, a VCC (=VL3) voltage is output to the segment-only pins and the segment/output port pins are the high impedance condition and pulled up to VCC (=VL3) voltage.

Also, the segment/I/O port pins(SEG26–SEG39) are set to input mode as I/O ports, and VCC (=VL3) is applied to them by pull-up resistor.

LCD Display RAM

Addresses 0040₁₆ to 0053₁₆ are the designated RAM for the LCD display. When “1” are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The frequency of internal signal LCDCK decided LCD drive timing and the frame frequency can be determined with the following equation:

$$f(\text{LCDCK}) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{\text{duty ratio}}$$

| Address \ Bit | Bit | | | | | | | |
|--------------------|------|------|-------|------|------|------|------|-------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | COM3 | COM2 | COM1 | COM0 | COM3 | COM2 | COM1 | COM0 |
| 0040 ₁₆ | | | SEG1 | | | | | SEG0 |
| 0041 ₁₆ | | | SEG3 | | | | | SEG2 |
| 0042 ₁₆ | | | SEG5 | | | | | SEG4 |
| 0043 ₁₆ | | | SEG7 | | | | | SEG6 |
| 0044 ₁₆ | | | SEG9 | | | | | SEG8 |
| 0045 ₁₆ | | | SEG11 | | | | | SEG10 |
| 0046 ₁₆ | | | SEG13 | | | | | SEG12 |
| 0047 ₁₆ | | | SEG15 | | | | | SEG14 |
| 0048 ₁₆ | | | SEG17 | | | | | SEG16 |
| 0049 ₁₆ | | | SEG19 | | | | | SEG18 |
| 004A ₁₆ | | | SEG21 | | | | | SEG20 |
| 004B ₁₆ | | | SEG23 | | | | | SEG22 |
| 004C ₁₆ | | | SEG25 | | | | | SEG24 |
| 004D ₁₆ | | | SEG27 | | | | | SEG26 |
| 004E ₁₆ | | | SEG29 | | | | | SEG28 |
| 004F ₁₆ | | | SEG31 | | | | | SEG30 |
| 0050 ₁₆ | | | SEG33 | | | | | SEG32 |
| 0051 ₁₆ | | | SEG35 | | | | | SEG34 |
| 0052 ₁₆ | | | SEG37 | | | | | SEG36 |
| 0053 ₁₆ | | | SEG39 | | | | | SEG38 |

Fig. 49 LCD display RAM map

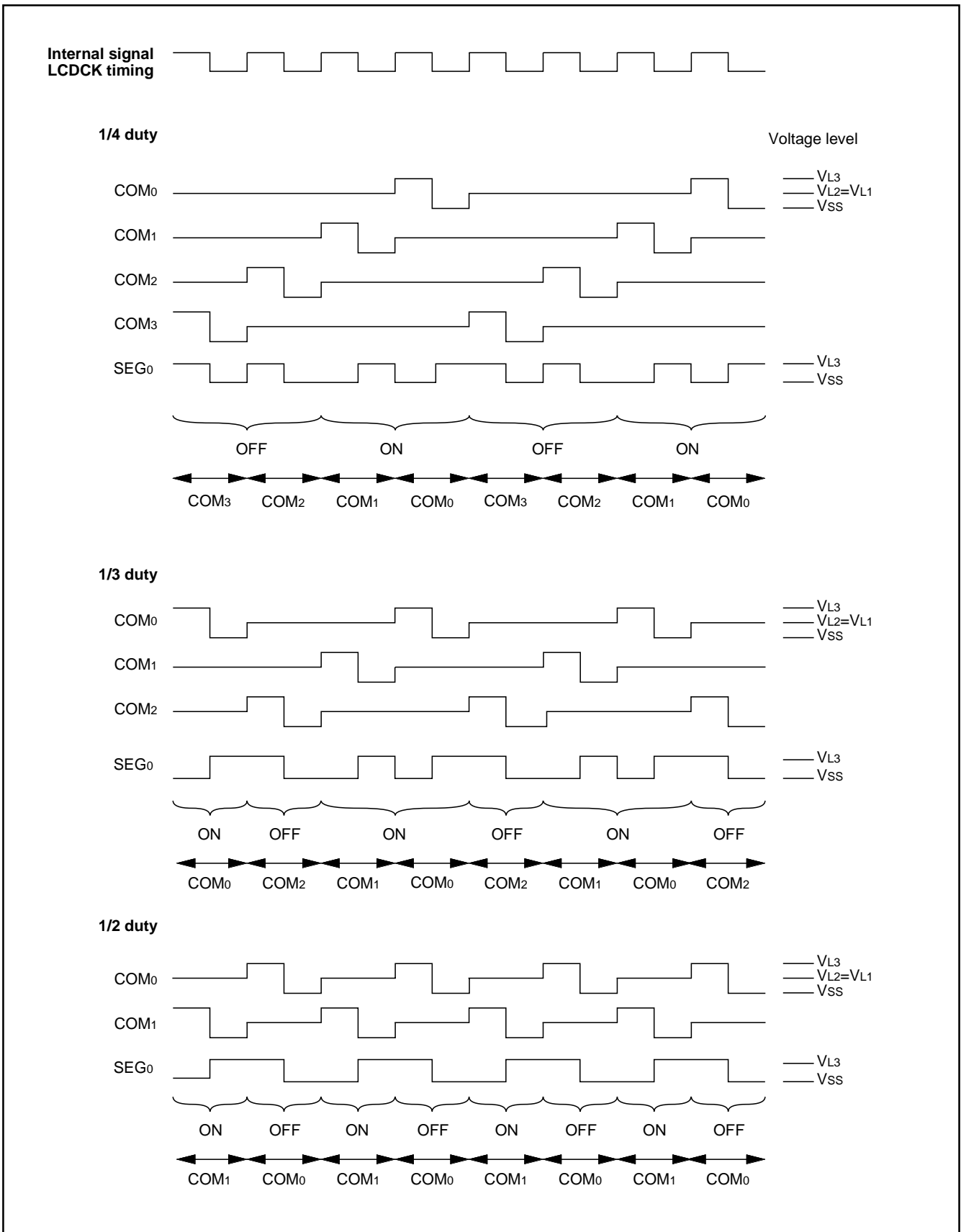


Fig. 50 LCD drive waveform (1/2 bias)

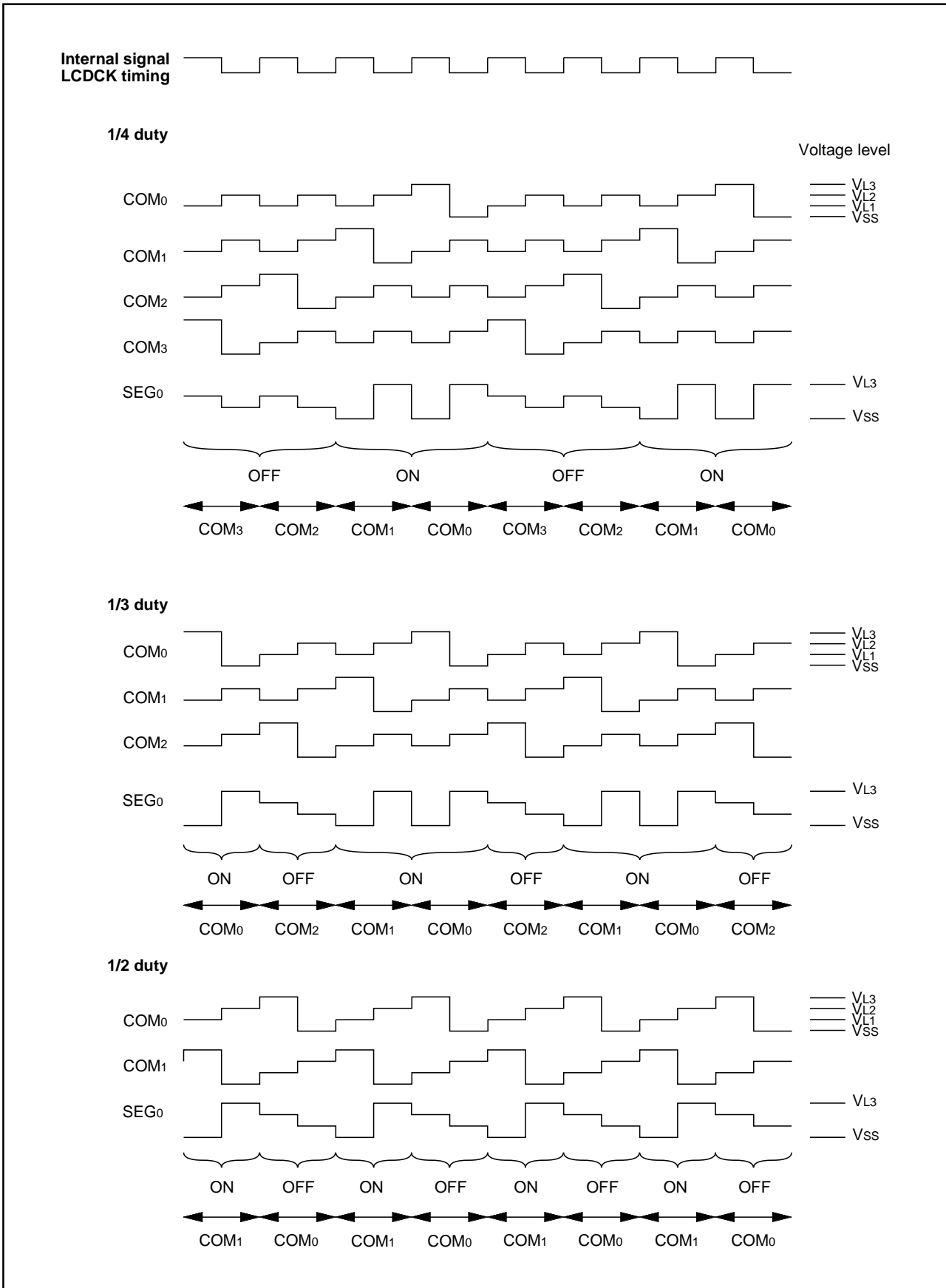


Fig. 51 LCD drive waveform (1/3 bias)

Watchdog Timer

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software runaway).

The watchdog timer consists of an 8-bit watchdog timer L and a 6-bit watchdog timer H. At reset or writing to the watchdog timer control register (address 0037₁₆), the watchdog timer is set to "3FFF₁₆". When any data is not written to the watchdog timer control register (address 0037₁₆) after reset, the watchdog timer is stopped. The watchdog timer starts to count down from "3FFF₁₆" by writing to the watchdog timer control register and an internal reset occurs at an underflow. Accordingly, when using the watchdog timer function, write the watchdog timer control register before an underflow. The watchdog timer does not function when writing to the watchdog timer control register has not been done after reset. When not using the watchdog timer, do not write to it. When the watchdog timer control register is read, the following values are read:

- value of high-order 6-bit counter
- value of STP instruction disable bit
- value of count source selection bit.

When the STP instruction disable bit is "0", the STP instruction is enabled. The STP instruction is disabled when this bit is set to "1". If the STP instruction which is disabled is executed, it is processed as an undefined instruction, so that a reset occurs internally.

This bit can be set to "1" but cannot be set to "0" by program. This bit is "0" after reset.

When the watchdog timer H count source selection bit is "0", the detection time is set to 8.19 s at $f(X_{CIN}) = 32 \text{ kHz}$ and 32.768 ms at $f(X_{IN}) = 8 \text{ MHz}$.

When the watchdog timer H count source selection bit is "1", the detection time is set to 32 ms at $f(X_{CIN}) = 32 \text{ kHz}$ and 128 μs at $f(X_{IN}) = 8 \text{ MHz}$. There is no difference in the detection time between the middle-speed mode and the high-speed mode.

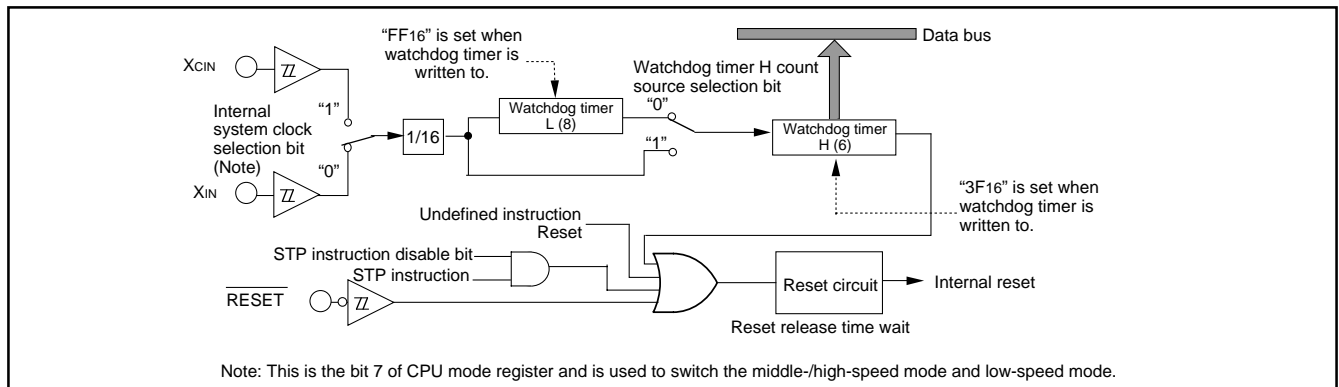


Fig. 52 Block diagram of watchdog timer

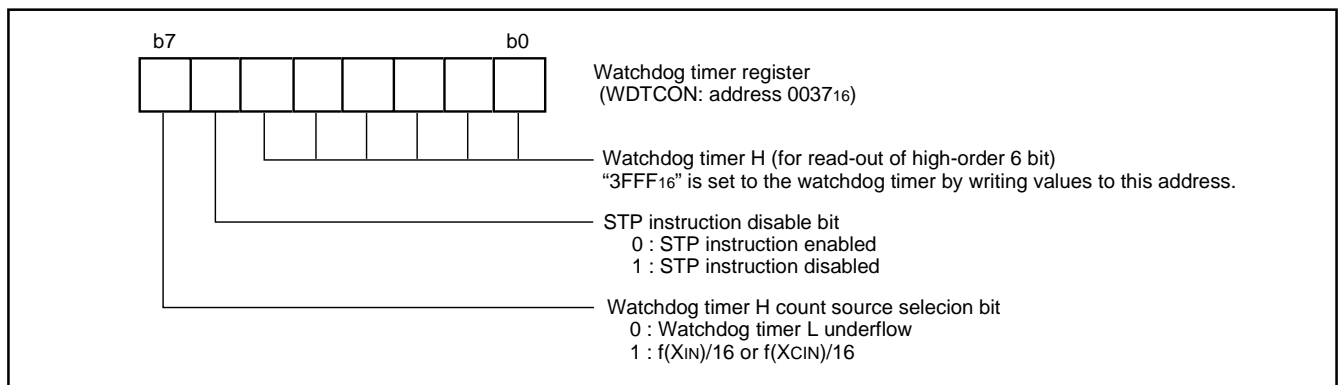


Fig. 53 Structure of watchdog timer control register

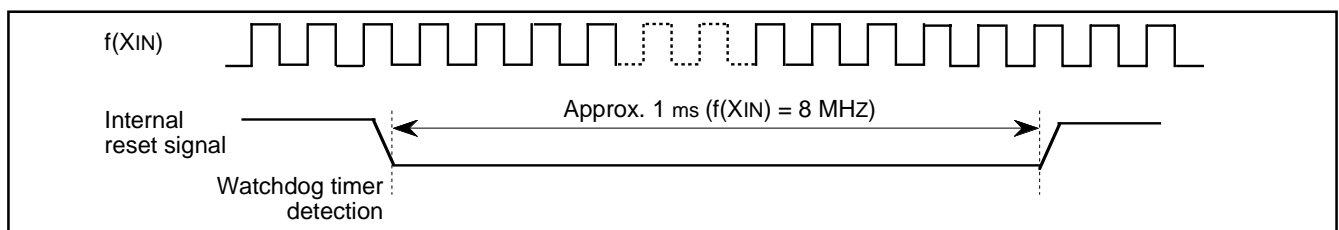


Fig. 54 Timing of reset output

TOUT/ ϕ OUTPUT FUNCTION

The system clock ϕ or timer 2 divided by 2 (TOUT output) can be output from port P43 by setting the TOUT/ ϕ output enable bit of the timer 123 mode register and the TOUT/ ϕ output control register. Set the P43/ ϕ /TOUT pin to output mode (set "1" to bit 3 of port P4 direction register) when outputting TOUT/ ϕ .

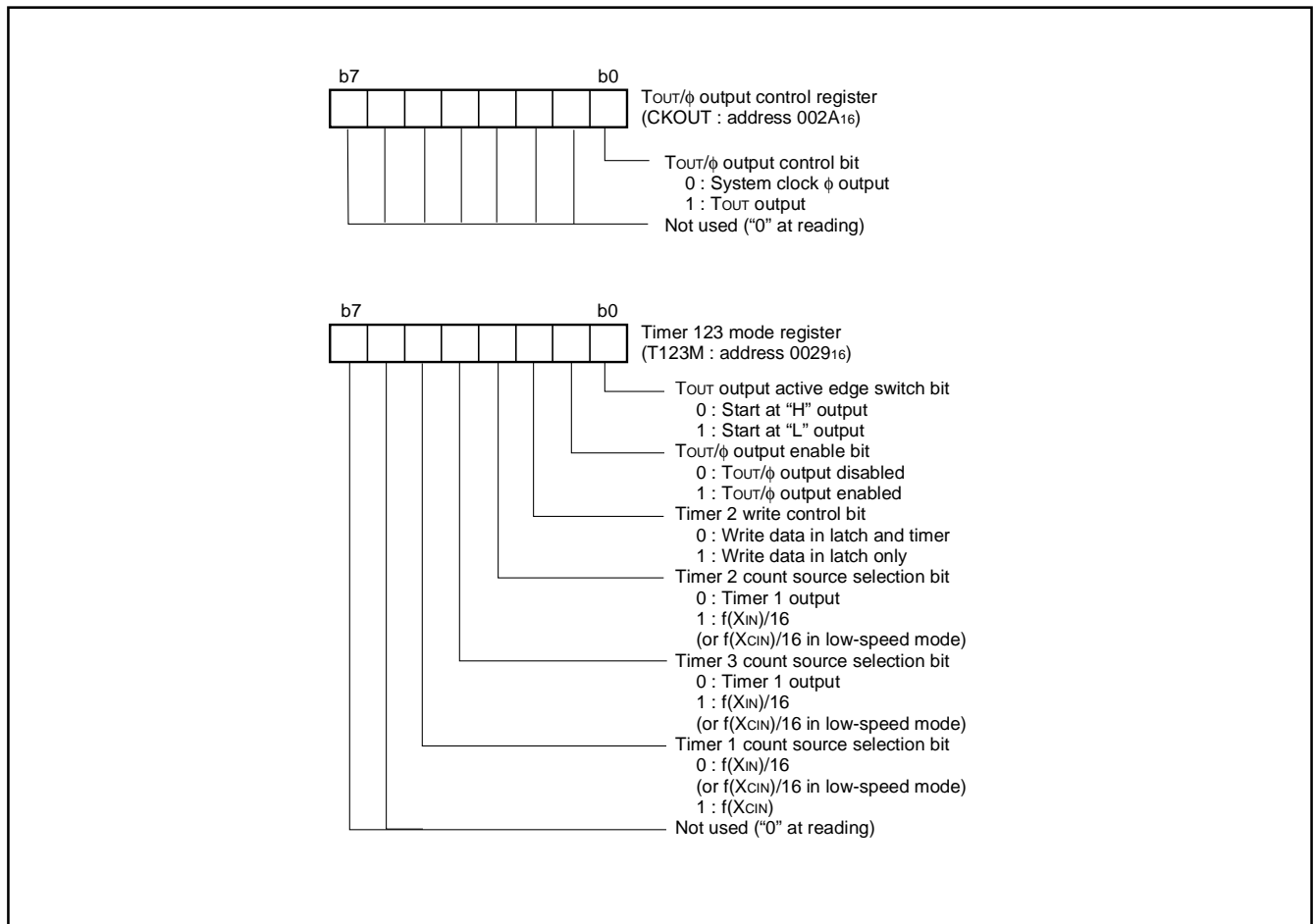


Fig. 55 Structure of TOUT/ ϕ output-related registers

RESET CIRCUIT

When the power source voltage is within limits, and main clock X_{IN}-X_{OUT} is stable, or a stabilized clock is input to the X_{IN} pin, if the $\overline{\text{RESET}}$ pin is held at an "L" level for 2 μs or more, the micro-computer is in an internal reset state. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level, reset is released after approximate 8200 cycles of f(X_{IN}), the program in address FFFD₁₆ (high-order byte)

and address FFFC₁₆ (low-order byte). Make sure that the reset input voltage is less than 0.2 V_{CC}(min.) for the power source voltage of V_{CC}(min.).

*V_{CC}(min.) = Minimum value of power supply voltage limits applied to V_{CC} pin

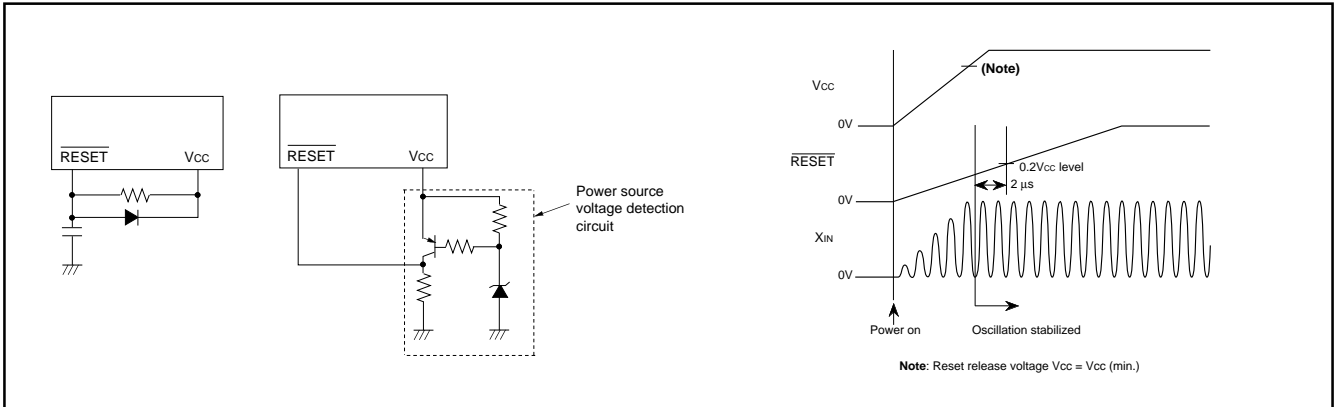


Fig. 56 Example of reset circuit

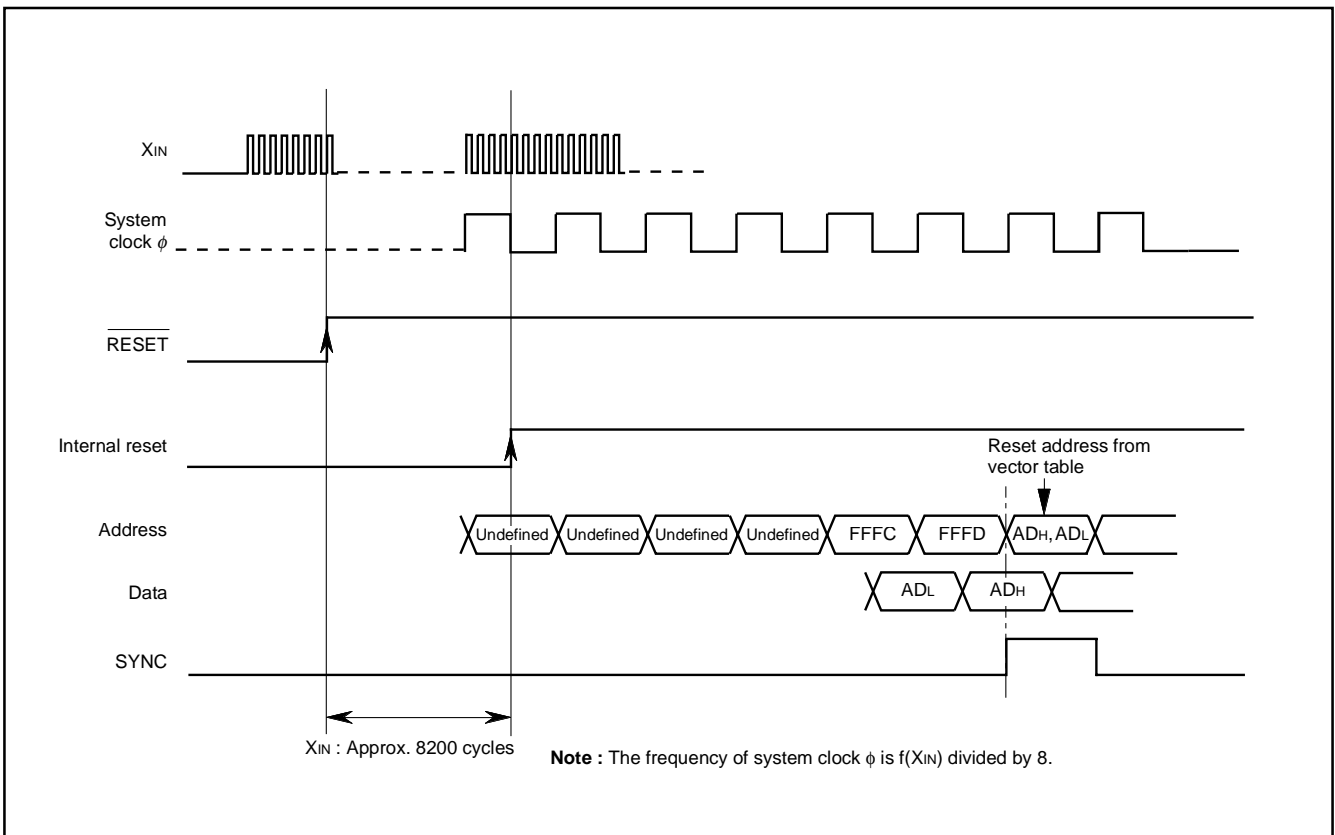


Fig. 57 Reset Sequence

| | Address | Register contents |
|--|--------------------|--|
| (1) Port P0 direction register | 0001 ₁₆ | 00 ₁₆ |
| (2) Port P1 direction register | 0003 ₁₆ | 00 ₁₆ |
| (3) Port P2 direction register | 0005 ₁₆ | 00 ₁₆ |
| (4) Port P3 output control register | 0007 ₁₆ | 00 ₁₆ |
| (5) Port P4 direction register | 0009 ₁₆ | 00 ₁₆ |
| (6) Port P5 direction register | 000B ₁₆ | 00 ₁₆ |
| (7) Port P6 direction register | 000D ₁₆ | 00 ₁₆ |
| (8) Port P7 direction register | 000F ₁₆ | 00 ₁₆ |
| (9) AD conversion low-order register | 0014 ₁₆ | X X 0 0 0 0 0 1 |
| (10) Key input control register | 0015 ₁₆ | 00 ₁₆ |
| (11) PULL register A | 0016 ₁₆ | 3F ₁₆ |
| (12) PULL register B | 0017 ₁₆ | 00 ₁₆ |
| (13) Serial I/O1 status register | 0019 ₁₆ | 1 0 0 0 0 0 0 0 |
| (14) Serial I/O1 control register | 001A ₁₆ | 00 ₁₆ |
| (15) UART control register | 001B ₁₆ | 1 1 1 0 0 0 0 0 |
| (16) Serial I/O2 control register | 001D ₁₆ | 00 ₁₆ |
| (17) Timer X low-order register | 0020 ₁₆ | FF ₁₆ |
| (18) Timer X high-order register | 0021 ₁₆ | FF ₁₆ |
| (19) Timer Y low-order register | 0022 ₁₆ | FF ₁₆ |
| (20) Timer Y high-order register | 0023 ₁₆ | FF ₁₆ |
| (21) Timer 1 register | 0024 ₁₆ | FF ₁₆ |
| (22) Timer 2 register | 0025 ₁₆ | 01 ₁₆ |
| (23) Timer 3 register | 0026 ₁₆ | FF ₁₆ |
| (24) Timer X mode register | 0027 ₁₆ | 00 ₁₆ |
| (25) Timer Y mode register | 0028 ₁₆ | 00 ₁₆ |
| (26) Timer 123 mode register | 0029 ₁₆ | 00 ₁₆ |
| (27) T _{OUT} /φ output control register | 002A ₁₆ | 00 ₁₆ |
| (28) PWM control register | 002B ₁₆ | 00 ₁₆ |
| (29) D-A1 conversion register | 0032 ₁₆ | 00 ₁₆ |
| (30) D-A2 conversion register | 0033 ₁₆ | 00 ₁₆ |
| (31) A-D control register | 0034 ₁₆ | 0 0 0 0 1 0 0 0 |
| (32) D-A control register | 0036 ₁₆ | 00 ₁₆ |
| (33) Watchdog timer control register | 0037 ₁₆ | 0 0 1 1 1 1 1 1 |
| (34) Segment output enable register | 0038 ₁₆ | 00 ₁₆ |
| (35) LCD mode register | 0039 ₁₆ | 00 ₁₆ |
| (36) Interrupt edge selection register | 003A ₁₆ | 00 ₁₆ |
| (37) CPU mode register | 003B ₁₆ | 0 1 0 0 1 0 0 0 |
| (38) Interrupt request register 1 | 003C ₁₆ | 00 ₁₆ |
| (39) Interrupt request register 2 | 003D ₁₆ | 00 ₁₆ |
| (40) Interrupt control register 1 | 003E ₁₆ | 00 ₁₆ |
| (41) Interrupt control register 2 | 003F ₁₆ | 00 ₁₆ |
| (42) Processor status register | (PS) | X X X X X 1 X X |
| (43) Program counter | (PC _H) | Contents of address FFFD ₁₆ |
| | (PC _L) | Contents of address FFFC ₁₆ |
| (44) Watchdog timer (high-order) | | 3F ₁₆ |
| (45) Watchdog timer (low-order) | | FF ₁₆ |

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
X : Undefined

Fig. 58 Internal state of microcomputer immediately after reset

CLOCK GENERATING CIRCUIT

The 7560 group has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub-clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting an oscillator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the oscillator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT since a resistor does not exist between them.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub-clock oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external oscillator to oscillate.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins go to high-impedance state.

Frequency Control

(1) Middle-speed mode

The clock input to the XIN pin is divided by 8 and it is used as the system clock ϕ .

After reset, this mode is selected.

(2) High-speed mode

The clock input to the XIN pin is divided by 2 and it is used as the system clock ϕ .

(3) Low-speed mode

- The clock input to the XCIN pin is divided by 2 and it is used as the system clock ϕ .

- A low-power consumption operation can be realized by stopping the main clock in this mode. To stop the main clock, set the main clock stop bit of the CPU mode register to "1".

When the main clock is restarted, after setting the main clock stop bit to "0", set enough time for oscillation to stabilize by program.

Note: If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency in the condition that $f(XIN) > 3 \cdot f(XCIN)$.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the system clock ϕ stops at an "H" level, and main and sub clock oscillators stop.

In this time, values set previously to timer 1 latch and timer 2 latch are loaded automatically to timer 1 and timer 2. Before the STP instruction, set the values to generate the wait time required for oscillation stabilization to timer 1 latch and timer 2 latch (low-order 8 bits are set to timer 1, high-order 8 bits are set to timer 2). Either $f(XIN)$ or $f(XCIN)$ divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2.

The bits of the timer 123 mode register except bit 4 are set to "0". Set the timer 1 and timer 2 interrupt enable bits to "0" before executing the STP instruction.

Oscillation restarts at reset or when an external interrupt is received, but the system clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize when a ceramic resonator is used.

(2) Wait mode

If the WIT instruction is executed, only the system clock ϕ stops at an "H" state. The states of main clock and sub clock are the same as the state before the executing the WIT instruction, and oscillation does not stop. Since supply of internal clock ϕ is started immediately after the interrupt is received, the instruction can be executed immediately.

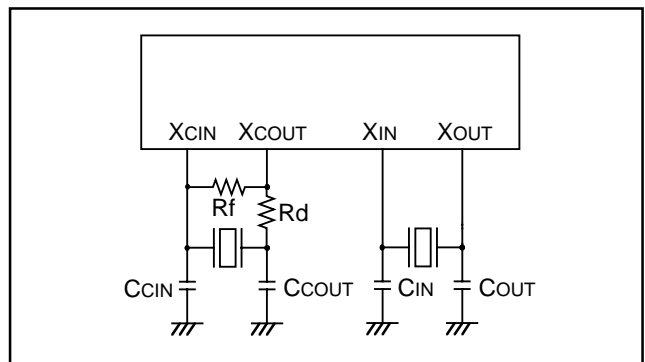


Fig. 59 Oscillator circuit

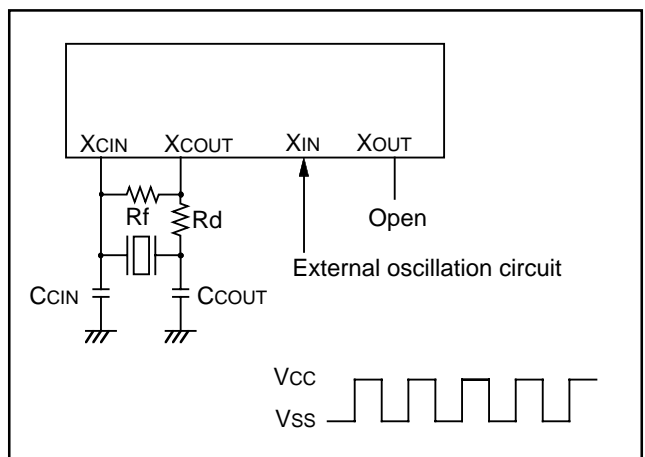


Fig. 60 External clock input circuit

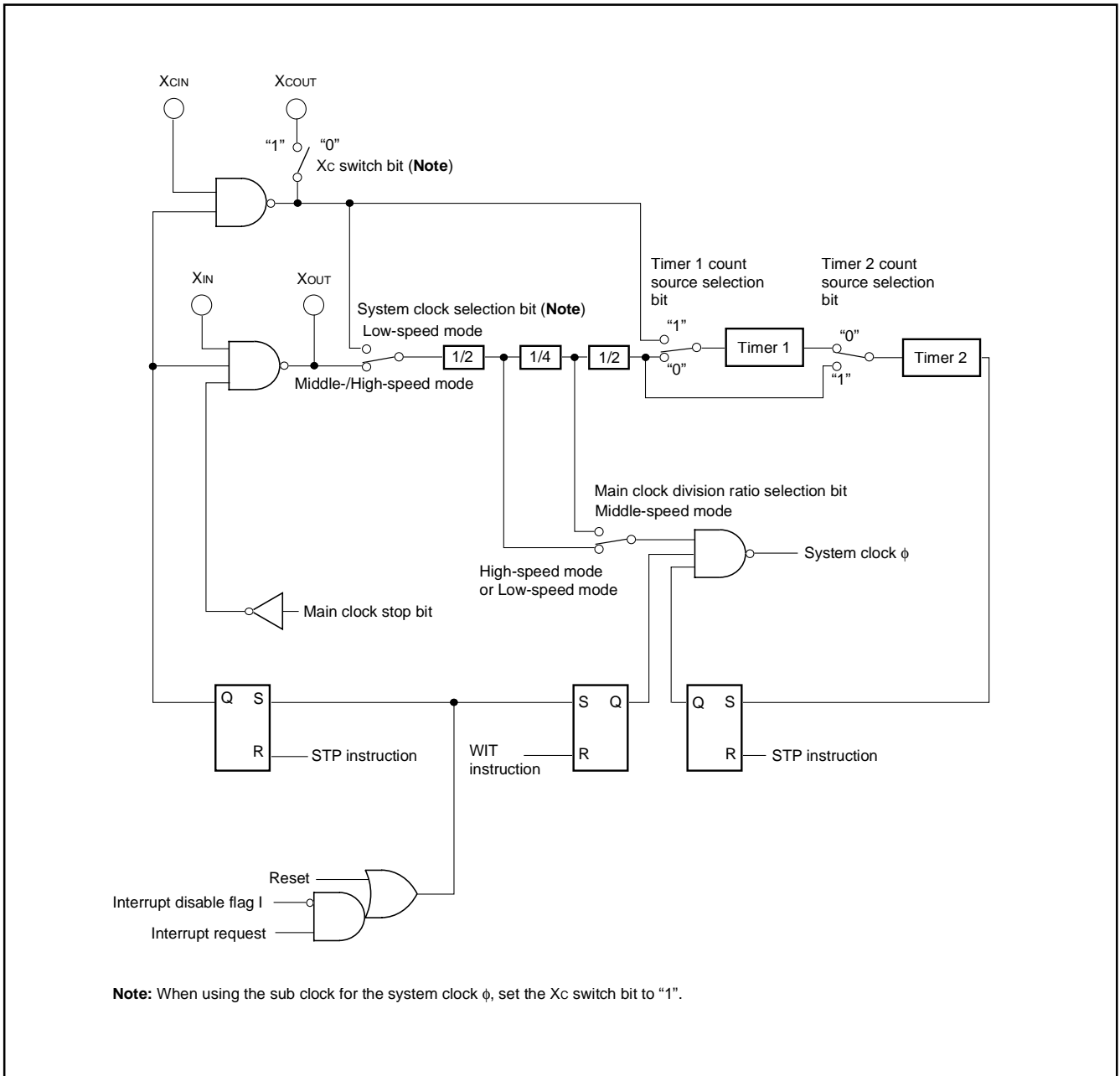


Fig. 61 Clock generating circuit block diagram

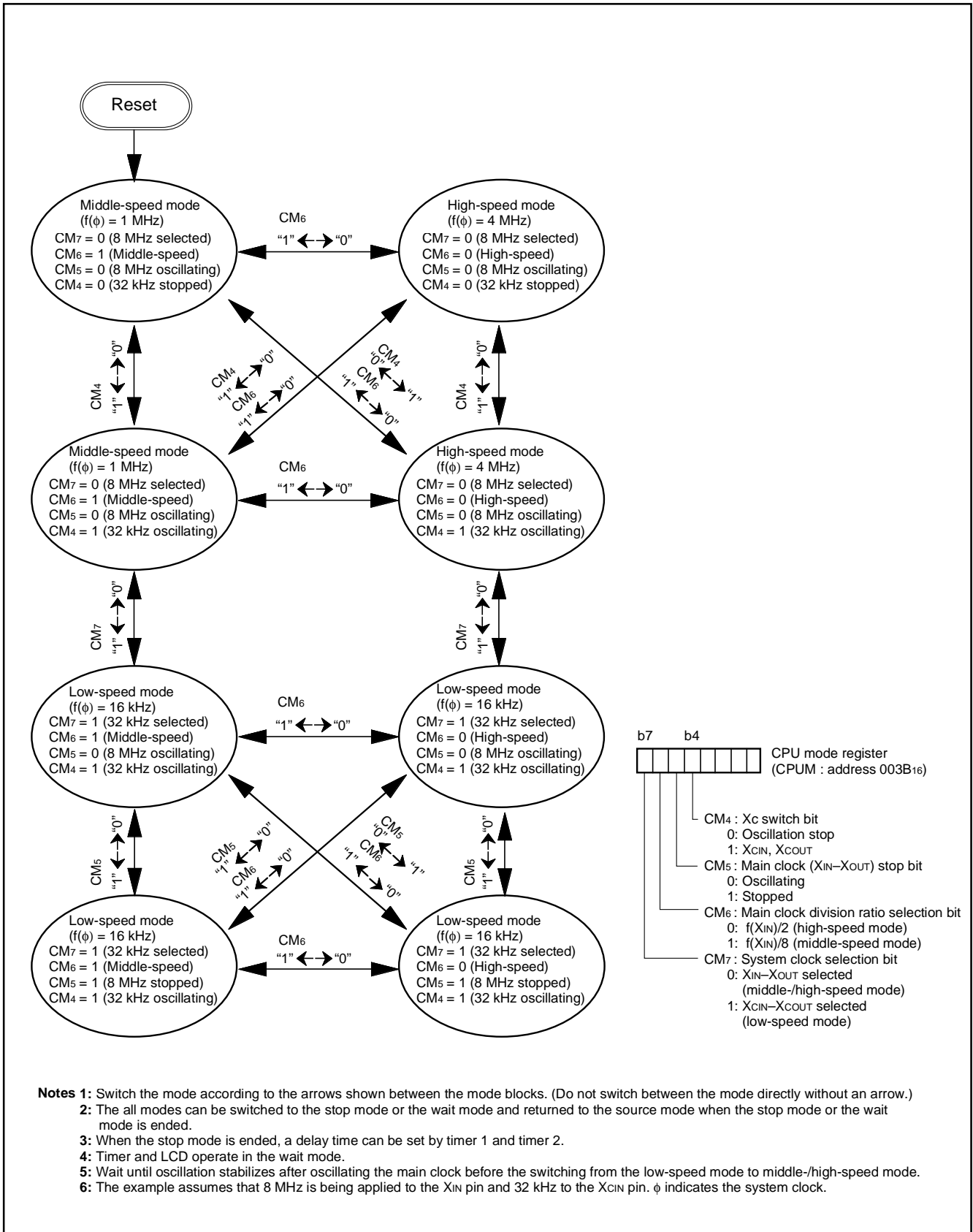


Fig. 62 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags (T flag, D flag, etc.) which affect program execution.

Interrupt

When the contents of an interrupt request bits are changed by the program, execute a BBC or BBS instruction after at least one instruction. This is for preventing executing a BBC or BBS instruction to the contents before change.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

Ports

Use instructions such as LDM and STA, etc., to set the port direction registers.

The contents of the port direction registers cannot be read.

The following cannot be used:

- LDA instruction
- The memory operation instruction when the T flag is "1"
- The bit-test instruction (BBC or BBS, etc.)
- The read-modify-write instruction (calculation instruction such as ROR etc., bit manipulation instruction such as CLB or SEB etc.)
- The addressing mode which uses the value of a direction register as an index

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".

The TxD pin of serial I/O1 retains the level then after transmission is completed.

In serial I/O2 selecting an internal clock, the SOUT2 pin goes to high impedance state after transmission is completed.

In serial I/O2 selecting an external clock, the SOUT2 pin retains the level then after transmission is completed.

A-D Converter

The input to the comparator is combined by internal capacitors. Therefore, since conversion accuracy may be worse by losing of an electric charge when the conversion speed is not enough, make sure that $f(\text{XIN})$ is at least 500 kHz during an A-D conversion.

The normal operation of A-D conversion cannot be guaranteed when performing the next operation:

- When writing to CPU mode register during A-D conversion operation
- When writing to A-D control register during A-D conversion operation
- When executing STP instruction or WIT instruction during A-D conversion operation

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the system clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the system clock ϕ depends on the main clock division ratio selection bit and the system clock selection bit.

NOTES ON USE
Countermeasures Against Noise

(1) Shortest wiring length

① Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20 mm).

● Reason

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

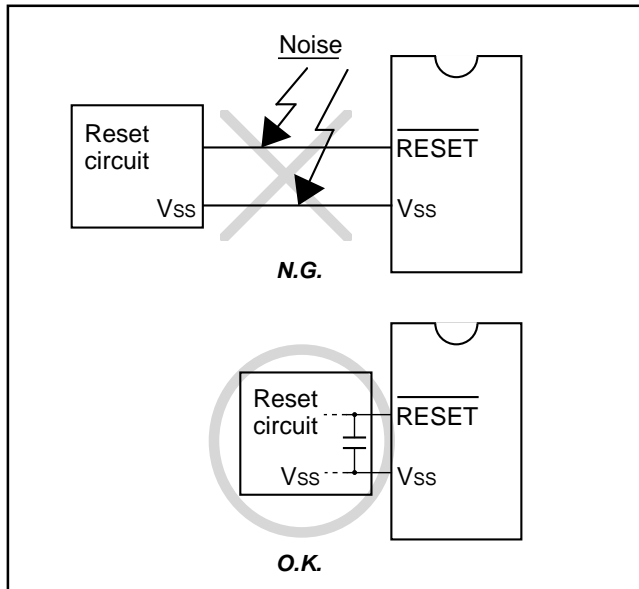


Fig. 63 Wiring for the $\overline{\text{RESET}}$ pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

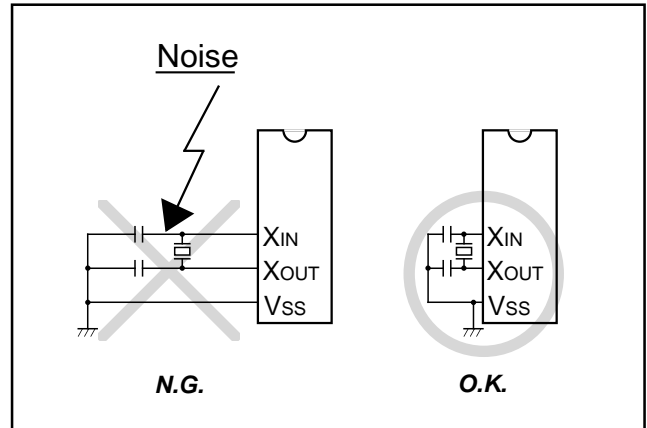


Fig. 64 Wiring for clock I/O pins

(2) Connection of bypass capacitor across Vss line and Vcc line
In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 μF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

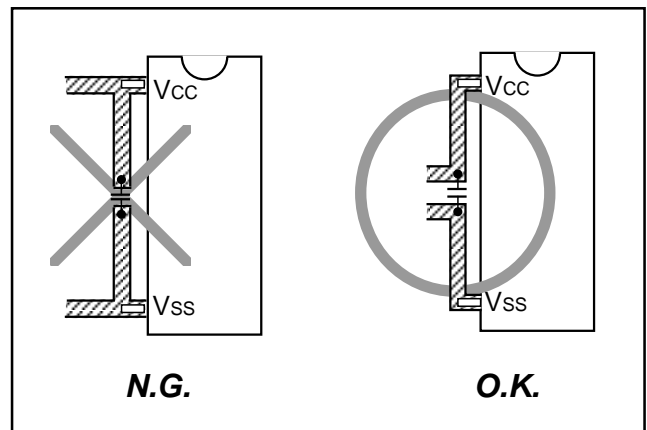


Fig. 65 Bypass capacitor across the Vss line and the Vcc line

(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of voltage or/and temperature is wide.

Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

① Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

② Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

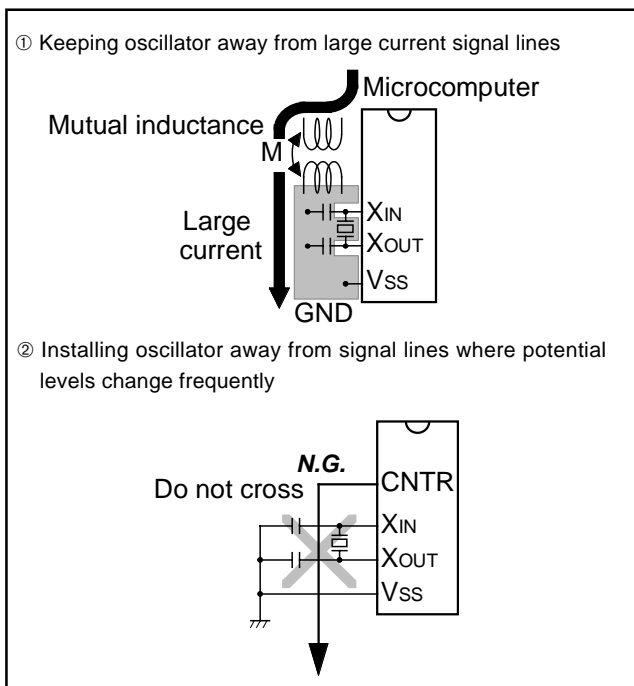


Fig. 66 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A-D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A-D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory type and size

When Mask ROM and PROM version and memory size differ in one group, actual values such as an electrical characteristics, A-D conversion accuracy, and the amount of proof of noise incorrect operation may differ from the ideal values.

When these products are used switching, perform system evaluation for each product of every after confirming product specification.

(6) Wiring to VPP pin of One Time PROM version and EPROM version

Connect an approximately 5 kΩ resistor to the VPP pin the shortest possible in series.

Note: Even when a circuit which included an approximately 5 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason

The VPP pin of the PROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for writing flow into the built-in PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

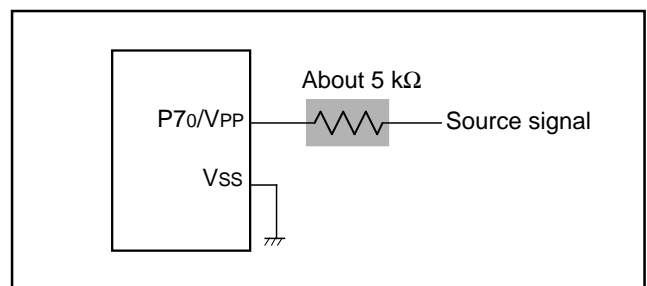


Fig. 67 Wiring for the VPP pin of One Time PROM

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- 1.Mask ROM Order Confirmation Form*
- 2.Mark Specification Form*
- 3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

*For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage (<http://www.infocom.maec.co.jp/indexe.htm>).

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 14 Special programming adapter

| Package | Name of Programming Adapter |
|----------|-----------------------------|
| 100P6S-A | PCA4738F-100A |
| 100P6Q-A | PCA4738G-100A |
| 100D0 | PCA4738L-100A |

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 68 is recommended to verify programming.

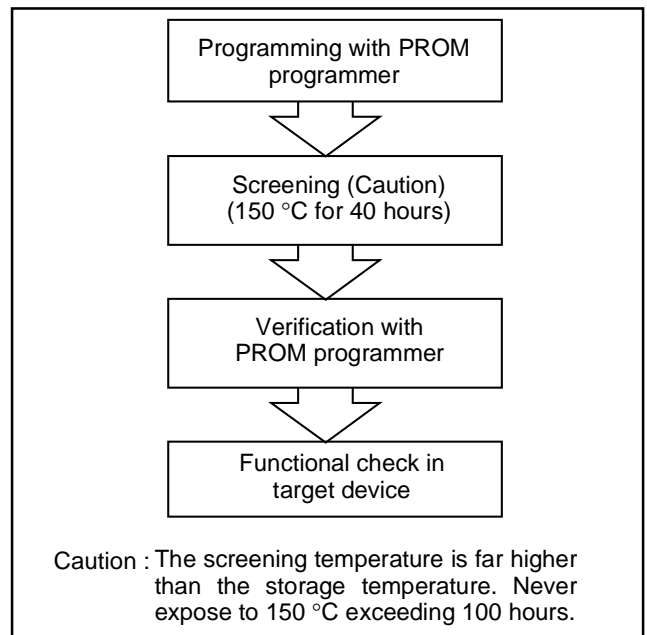


Fig. 68 State transitions of system clock

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

Table 15 Absolute maximum ratings

| Symbol | Parameter | Conditions | Ratings | Unit | |
|--------|--|---|-------------------|-------------|---|
| VCC | Power source voltage | All voltages are based on VSS. Output transistors are cut off. | -0.3 to 6.5 | V | |
| VI | Input voltage P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67 | | -0.3 to VCC +0.3 | V | |
| VI | Input voltage P70-P77 | | -0.3 to VCC +0.3 | V | |
| VI | Input voltage VL1 | | -0.3 to VL2 | V | |
| VI | Input voltage VL2 | | VL1 to VL3 | V | |
| VI | Input voltage VL3 | | VL2 to 6.5 | V | |
| VI | Input voltage C1, C2 | | -0.3 to 6.5 | V | |
| VI | Input voltage RESET, XIN | | -0.3 to VCC +0.3 | V | |
| VO | Output voltage C1, C2 | | -0.3 to 6.5 | V | |
| VO | Output voltage P00-P07, P10-P15, P30-P37 | | At output port | -0.3 to VCC | V |
| | | | At segment output | -0.3 to VL3 | V |
| VO | Output voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77 | | -0.3 to VCC +0.3 | V | |
| VO | Output voltage VL3 | | -0.3 to 6.5 | V | |
| VO | Output voltage VL2, SEG0-SEG17 | | -0.3 to VL3 | V | |
| VO | Output voltage XOUT | | -0.3 to VCC +0.3 | V | |
| Pd | Power dissipation | Ta = 25°C | 300 | mW | |
| Topr | Operating temperature | | -20 to 85 | °C | |
| Tstg | Storage temperature | | -40 to 125 | °C | |

RECOMMENDED OPERATING CONDITIONS

Table 16 Recommended operating conditions (1) (VCC = 2.2 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit | |
|--------|---------------------------------------|----------------------------------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| VCC | Power source voltage | High-speed mode f(XIN) = 8 MHz | 4.0 | 5.0 | 5.5 | V |
| | | Middle-speed mode f(XIN) = 8 MHz | 2.2 | 5.0 | 5.5 | |
| | | Low-speed mode | 2.2 | 5.0 | 5.5 | |
| VSS | Power source voltage | | 0 | | V | |
| VREF | A-D, D-A conversion reference voltage | 2.0 | | VCC | V | |
| AVSS | Analog power source voltage | | 0 | | V | |
| VIA | Analog input voltage AN0-AN7 | AVSS | | VCC | V | |

Table 17 Recommended operating conditions (2) (V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|-----------------|-------------------|---|---------------------|------|---------------------|------|
| | | | Min. | Typ. | Max. | |
| V _{IH} | "H" input voltage | P00-P07, P10-P17, P40, P43, P45, P47, P50-P53, P56, P61, P64-P67, P71-P77 | 0.7 V _{CC} | | V _{CC} | V |
| V _{IH} | "H" input voltage | P20-P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70 | 0.8 V _{CC} | | V _{CC} | V |
| V _{IH} | "H" input voltage | RESET | 0.8 V _{CC} | | V _{CC} | V |
| V _{IH} | "H" input voltage | X _{IN} | 0.8 V _{CC} | | V _{CC} | V |
| V _{IL} | "L" input voltage | P00-P07, P10-P17, P40, P43, P45, P47, P50-P53, P56, P61, P64-P67, P71-P77 | 0 | | 0.3 V _{CC} | V |
| V _{IL} | "L" input voltage | P20-P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70 | 0 | | 0.2 V _{CC} | V |
| V _{IL} | "L" input voltage | RESET | 0 | | 0.2 V _{CC} | V |
| V _{IL} | "L" input voltage | X _{IN} | 0 | | 0.2 V _{CC} | V |

Table 18 Recommended operating conditions (3) (V_{CC} = 2.2 to 2.5 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|-----------------|-------------------|---|----------------------|------|----------------------|------|
| | | | Min. | Typ. | Max. | |
| V _{IH} | "H" input voltage | P00-P07, P10-P17, P40, P43, P45, P47, P50-P53, P56, P61, P64-P67, P71-P77 | 0.8 V _{CC} | | V _{CC} | V |
| V _{IH} | "H" input voltage | P20-P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70 | 0.95 V _{CC} | | V _{CC} | V |
| V _{IH} | "H" input voltage | RESET | 0.95 V _{CC} | | V _{CC} | V |
| V _{IH} | "H" input voltage | X _{IN} | 0.95 V _{CC} | | V _{CC} | V |
| V _{IL} | "L" input voltage | P00-P07, P10-P17, P40, P43, P45, P47, P50-P53, P56, P61, P64-P67, P71-P77 | 0 | | 0.2 V _{CC} | V |
| V _{IL} | "L" input voltage | P20-P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70 | 0 | | 0.05 V _{CC} | V |
| V _{IL} | "L" input voltage | RESET | 0 | | 0.05 V _{CC} | V |
| V _{IL} | "L" input voltage | X _{IN} | 0 | | 0.05 V _{CC} | V |

Table 19 Recommended operating conditions (4) (Vcc = 2.2 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| ΣIOH(peak) | "H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | -20 | mA |
| ΣIOH(peak) | "H" total peak output current P41-P47, P50-P57, P60-P67 (Note 1) | | | -20 | mA |
| ΣIOL(peak) | "L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | 20 | mA |
| ΣIOL(peak) | "L" total peak output current P41-P47, P50-P57, P60-P67 (Note 1) | | | 20 | mA |
| ΣIOL(peak) | "L" total peak output current P40, P71-P77 (Note 1) | | | 80 | mA |
| ΣIOH(avg) | "H" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | -10 | mA |
| ΣIOH(avg) | "H" total average output current P41-P47, P50-P57, P60-P67 (Note 1) | | | -10 | mA |
| ΣIOL(avg) | "L" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | 10 | mA |
| ΣIOL(avg) | "L" total average output current P41-P47, P50-P57, P60-P67 (Note 1) | | | 10 | mA |
| ΣIOL(avg) | "L" total average output current P40, P71-P77 (Note 1) | | | 40 | mA |
| IOH(peak) | "H" peak output current P00-P07, P10-P15, P30-P37 (Note 2) | | | -1.0 | mA |
| IOH(peak) | "H" peak output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 2) | | | -5.0 | mA |
| IOL(peak) | "L" peak output current P00-P07, P10-P15, P30-P37 (Note 2) | | | 5.0 | mA |
| IOL(peak) | "L" peak output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 2) | | | 10 | mA |
| IOL(peak) | "L" peak output current P40, P71-P77 (Note 2) | | | 20 | mA |
| IOH(avg) | "H" average output current P00-P07, P10-P15, P30-P37 (Note 3) | | | -0.5 | mA |
| IOH(avg) | "H" average output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 3) | | | -2.5 | mA |
| IOL(avg) | "L" average output current P00-P07, P10-P15, P30-P37 (Note 3) | | | 2.5 | mA |
| IOL(avg) | "L" average output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 3) | | | 5.0 | mA |
| IOL(avg) | "L" average output current P40, P71-P77 (Note 3) | | | 10 | mA |

Notes1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

Table 20 Recommended operating conditions (5) ($V_{CC} = 2.2$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------------|---|---|--------|--------|----------------------------|------|
| | | | Min. | Typ. | Max. | |
| f(CNTR0) f(CNTR1) | Input frequency for timers X and Y (duty cycle 50%) | $(4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V})$ | | | 4.0 | MHz |
| | | $(V_{CC} \leq 4.0\text{ V})$ | | | $(10 \times V_{CC} - 4)/9$ | MHz |
| f(XIN) | Main clock input oscillation frequency (Note 1) | High-speed mode $(4.0\text{ V} \leq V_{CC} \leq 5.5\text{ V})$ | | | 8.0 | MHz |
| | | High-speed mode $(2.2\text{ V} \leq V_{CC} \leq 4.0\text{ V})$ | | | $(20 \times V_{CC} - 8)/9$ | MHz |
| | | Middle-speed mode | | | 8.0 | MHz |
| f(XCIN) | Sub-clock input oscillation frequency (Notes 1, 2) | | | 32.768 | 50 | kHz |

Notes1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(XCIN) < f(XIN)/3$.

Table 21 Electrical characteristics (1) (Vcc =4.0 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------|---|--|---------|--------|--------|------|
| | | | Min. | Typ. | Max. | |
| VOH | "H" output voltage P00-P07, P10-P15, P30-P37 | IOH = -1 mA | Vcc-2.0 | | | V |
| | | IOH = -0.25 mA Vcc = 2.2 V | Vcc-0.8 | | | V |
| VOH | "H" output voltage P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 1) | IOH = -5 mA | Vcc-2.0 | | | V |
| | | IOH = -1.5 mA | Vcc-0.5 | | | V |
| | | IOH = -1.25 mA Vcc = 2.2 V | Vcc-0.8 | | | V |
| VOL | "L" output voltage P00-P07, P10-P15, P30-P37 | IOl = 5 mA | | | 2.0 | V |
| | | IOl = 1.5 mA | | | 0.5 | V |
| | | IOl = 1.25 mA Vcc = 2.2 V | | | 0.8 | V |
| VOL | "L" output voltage P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 | IOl = 10 mA | | | 2.0 | V |
| | | IOl = 3.0 mA | | | 0.5 | V |
| | | IOl = 2.5 mA Vcc = 2.2 V | | | 0.8 | V |
| VOL | "L" output voltage P40, P71-P77 | IOl = 10 mA | | | 0.5 | V |
| | | IOl = 5 mA Vcc = 2.2 V | | | 0.3 | V |
| VT+ - VT- | Hysteresis INT0-INT2, ADT, CNTR0, CNTR1, P20-P27 | | | 0.5 | | V |
| VT+ - VT- | Hysteresis SCLK, RXD, SIN2 | | | 0.5 | | V |
| VT+ - VT- | Hysteresis RESET | | | 0.5 | | V |
| IiH | "H" input current P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67, P70-P77 | Vi = Vcc | | | 5.0 | μA |
| IiH | "H" input current RESET | Vi = Vcc | | | 5.0 | μA |
| IiH | "H" input current XIN | Vi = Vcc | | 4.0 | | μA |
| IiL | "L" input current P00-P07, P10-P17, P20-P27, P41-P47, P50-P57, P60-P67 | Vi = Vss Pull-ups "off" | | | -5.0 | μA |
| | | Vcc = 5 V, Vi = Vss Pull-ups "on" | -60.0 | -120.0 | -240.0 | μA |
| | | Vcc = 2.2 V, Vi = Vss Pull-ups "on" | -5.0 | -20.0 | -40.0 | μA |
| IiL | "L" input current P40, P70-P77 | | | | -5.0 | μA |
| IiL | "L" input current RESET | Vi = Vss | | | -5.0 | μA |
| IiL | "L" input current XIN | Vi = Vss | | -4.0 | | μA |
| ILOAD | Output load current P30-P37 | Vcc = 5.0 V, Vo = Vcc, Pullup ON Output transistors "off" | -60.0 | -120.0 | -240.0 | μA |
| | | Vcc = 2.2 V, Vo = Vcc, Pullup ON Output transistors "off" | -5.0 | -20.0 | -40.0 | μA |
| Ileak | Output leak current P30-P37 | Vo = Vcc, Pullup OFF Output transistors "off" | | | 5.0 | μA |
| | | Vo = Vss, Pullup OFF Output transistors "off" | | | -5.0 | μA |

Table 22 Electrical characteristics (2) (V_{CC} = 2.2 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit | |
|-----------------|--|--|------------------------|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| VRAM | RAM retention voltage | At clock stop mode | 2.0 | | 5.5 | V | |
| I _{CC} | Power source current | <ul style="list-style-type: none"> High-speed mode, V_{CC} = 5 V f(X_{IN}) = 8 MHz f(X_{CIN}) = 32.768 kHz Output transistors "off" A-D converter in operating | | 6.4 | 13 | mA | |
| | | <ul style="list-style-type: none"> High-speed mode, V_{CC} = 5 V f(X_{IN}) = 8 MHz (in WIT state) f(X_{CIN}) = 32.768 kHz Output transistors "off" A-D converter stop | | 1.6 | 3.2 | mA | |
| | | <ul style="list-style-type: none"> Low-speed mode, V_{CC} = 5 V, T_a ≤ 55°C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz Output transistors "off" | | 35 | 70 | μA | |
| | | <ul style="list-style-type: none"> Low-speed mode, V_{CC} = 5 V, T_a = 25°C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz (in WIT state) Output transistors "off" | | 20 | 40 | μA | |
| | | <ul style="list-style-type: none"> Low-speed mode, V_{CC} = 3 V, T_a ≤ 55°C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz Output transistors "off" | | 15 | 22 | μA | |
| | | <ul style="list-style-type: none"> Low-speed mode, V_{CC} = 3 V, T_a = 25°C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz (in WIT state) Output transistors "off" | | 4.5 | 9.0 | μA | |
| | | All oscillation stopped (in STP state) Output transistors "off" | T _a = 25 °C | | 0.1 | 1.0 | μA |
| | | | T _a = 85 °C | | | 10 | |
| VL1 | Power source voltage | When using voltage multiplier | 1.3 | 1.8 | 2.1 | V | |
| IL1 | Power source current (VL1) (Note) | VL1 = 1.8 V | | 4.0 | | μA | |

Note: When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".

Table 23 A-D converter characteristics

(VCC = 2.7 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85°C, f(XIN) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)
 8-bit A-D mode (when conversion mode selection bit (bit 0 of address 001416) is "1")

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---------|--|---------------------------|--------|------|------|---------------------|
| | | | Min. | Typ. | Max. | |
| - | Resolution | | | | 8 | Bits |
| - | Absolute accuracy (excluding quantization error) | VCC = VREF = 2.7 to 5.5 V | | | ±2 | LSB |
| tCONV | Conversion time | | 49 | | 50 | tc(ADCLK) (Note) |
| RLADDER | Ladder resistor | | 12 | 35 | 100 | kΩ |
| IVREF | Reference power source input current | VREF = 5 V | 50 | 150 | 200 | μA |
| IIA | Analog port input current | | | | 5.0 | μA |

Note: ADCLK is the control clock of the A-D converter. System clock φ is used.

Table 24 A-D converter characteristics

(VCC = 2.7 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85°C, f(XIN) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)
 10-bit A-D mode (when conversion mode selection bit (bit 0 of address 001416) is "0")

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---------|--|---------------------------|--------|------|------|---------------------|
| | | | Min. | Typ. | Max. | |
| - | Resolution | | | | 10 | Bits |
| - | Absolute accuracy (excluding quantization error) | VCC = VREF = 2.7 to 5.5 V | | | ±4 | LSB |
| tCONV | Conversion time | | 61 | | 62 | tc(ADCLK) (Note) |
| RLADDER | Ladder resistor | | 12 | 35 | 100 | kΩ |
| IVREF | Reference power source input current | VREF = 5 V | 50 | 150 | 200 | μA |
| IIA | Analog port input current | | | | 5.0 | μA |

Note: ADCLK is the control clock of the A-D converter. System clock φ is used.

Table 25 D-A converter characteristics

(VCC = 2.7 to 5.5 V, VCC = VREF, VSS = AVSS = 0 V, Ta = -20 to 85°C, in middle/high-speed mode unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|--------|--------------------------------------|--------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| - | Resolution | | | | 8 | Bits |
| - | Absolute accuracy | VCC = VREF = 5 V | | | 1.0 | % |
| | | VCC = VREF = 2.7 V | | | 2.0 | % |
| tsu | Setting time | | | 3 | | μs |
| RO | Output resistor | | 1 | 2.5 | 4 | kΩ |
| IVREF | Reference power source input current | (Note) | | | 3.2 | mA |

Note: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.

Table 26 Timing requirements 1 (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|--|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _w (RESET) | Reset input "L" pulse width | 2 | | | μs |
| t _c (X _{IN}) | Main clock input cycle time (X _{IN} input) | 125 | | | ns |
| t _{wH} (X _{IN}) | Main clock input "H" pulse width | 45 | | | ns |
| t _{wL} (X _{IN}) | Main clock input "L" pulse width | 40 | | | ns |
| t _c (CNTR) | CNTR ₀ , CNTR ₁ input cycle time | 250 | | | ns |
| t _{wH} (CNTR) | CNTR ₀ , CNTR ₁ input "H" pulse width | 105 | | | ns |
| t _{wL} (CNTR) | CNTR ₀ , CNTR ₁ input "L" pulse width | 105 | | | ns |
| t _{wH} (INT) | INT ₀ to INT ₂ input "H" pulse width | 80 | | | ns |
| t _{wL} (INT) | INT ₀ to INT ₂ input "L" pulse width | 80 | | | ns |
| t _c (SCLK ₁) | Serial I/O1 clock input cycle time (Note) | 800 | | | ns |
| t _{wH} (SCLK ₁) | Serial I/O1 clock input "H" pulse width (Note) | 370 | | | ns |
| t _{wL} (SCLK ₁) | Serial I/O1 clock input "L" pulse width (Note) | 370 | | | ns |
| t _{su} (RxD–SCLK ₁) | Serial I/O1 input set up time | 220 | | | ns |
| t _h (SCLK ₁ –RxD) | Serial I/O1 input hold time | 100 | | | ns |
| t _c (SCLK ₂) | Serial I/O2 clock input cycle time (Note) | 1000 | | | ns |
| t _{wH} (SCLK ₂) | Serial I/O2 clock input "H" pulse width (Note) | 400 | | | ns |
| t _{wL} (SCLK ₂) | Serial I/O2 clock input "L" pulse width (Note) | 400 | | | ns |
| t _{su} (S _{IN2} –SCLK ₂) | Serial I/O2 input set up time | 200 | | | ns |
| t _h (SCLK ₂ –S _{IN2}) | Serial I/O2 input hold time | 200 | | | ns |

Note: When bit 6 of address 001A₁₆ is "1".

Divide this value by four when bit 6 of address 001A₁₆ is "0".

Table 27 Timing requirements 2 (V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|--|---|----------------------------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _w (RESET) | Reset input "L" pulse width | 2 | | | μs |
| t _c (X _{IN}) | Main clock input cycle time (X _{IN} input) | 125 | | | ns |
| t _{wH} (X _{IN}) | Main clock input "H" pulse width | 45 | | | ns |
| t _{wL} (X _{IN}) | Main clock input "L" pulse width | 40 | | | ns |
| t _c (CNTR) | CNTR ₀ , CNTR ₁ input cycle time | 900/(V _{CC} -0.4) | | | ns |
| t _{wH} (CNTR) | CNTR ₀ , CNTR ₁ input "H" pulse width | t _c (CNTR)/2–20 | | | ns |
| t _{wL} (CNTR) | CNTR ₀ , CNTR ₁ input "L" pulse width | t _c (CNTR)/2–20 | | | ns |
| t _{wH} (INT) | INT ₀ to INT ₂ input "H" pulse width | 230 | | | ns |
| t _{wL} (INT) | INT ₀ to INT ₂ input "L" pulse width | 230 | | | ns |
| t _c (SCLK ₁) | Serial I/O1 clock input cycle time (Note) | 2000 | | | ns |
| t _{wH} (SCLK ₁) | Serial I/O1 clock input "H" pulse width (Note) | 950 | | | ns |
| t _{wL} (SCLK ₁) | Serial I/O1 clock input "L" pulse width (Note) | 950 | | | ns |
| t _{su} (RxD–SCLK ₁) | Serial I/O1 input set up time | 400 | | | ns |
| t _h (SCLK ₁ –RxD) | Serial I/O1 input hold time | 200 | | | ns |
| t _c (SCLK ₂) | Serial I/O2 clock input cycle time (Note) | 2000 | | | ns |
| t _{wH} (SCLK ₂) | Serial I/O2 clock input "H" pulse width (Note) | 950 | | | ns |
| t _{wL} (SCLK ₂) | Serial I/O2 clock input "L" pulse width (Note) | 950 | | | ns |
| t _{su} (S _{IN2} –SCLK ₂) | Serial I/O2 input set up time | 400 | | | ns |
| t _h (SCLK ₂ –S _{IN2}) | Serial I/O2 input hold time | 300 | | | ns |

Note: When bit 6 of address 001A₁₆ is "1".

Divide this value by four when bit 6 of address 001A₁₆ is "0".

Table 28 Switching characteristics 1 (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------------------------|--|------------------------------|------|------------------------------|------|
| | | Min. | Typ. | Max. | |
| t _{wH} (SCLK1) | Serial I/O1 clock output "H" pulse width | t _c (SCLK1)/2-30 | | | ns |
| t _{wL} (SCLK1) | Serial I/O1 clock output "L" pulse width | t _c (SCLK1)/2-30 | | | ns |
| t _d (SCLK1-TxD) | Serial I/O1 output delay time (Note 1) | | | 140 | ns |
| t _v (SCLK1-TxD) | Serial I/O1 output valid time (Note 1) | -30 | | | ns |
| t _r (SCLK1) | Serial I/O1 clock output rising time | | | 30 | ns |
| t _f (SCLK1) | Serial I/O1 clock output falling time | | | 30 | ns |
| t _{wH} (SCLK2) | Serial I/O2 clock output "H" pulse width | t _c (SCLK2)/2-160 | | | ns |
| t _{wL} (SCLK2) | Serial I/O2 clock output "L" pulse width | t _c (SCLK2)/2-160 | | | ns |
| t _d (SCLK2-SOUT2) | Serial I/O2 output delay time | | | 0.2 X t _c (SCLK2) | ns |
| t _v (SCLK2-SOUT2) | Serial I/O2 output valid time | 0 | | | ns |
| t _f (SCLK2) | Serial I/O2 clock output falling time | | | 40 | ns |
| t _r (CMOS) | CMOS output rising time (Note 2) | | 10 | 30 | ns |
| t _f (CMOS) | CMOS output falling time (Note 2) | | 10 | 30 | ns |

Notes1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".
2: XOUT and XCOU pins are excluded.

Table 29 Switching characteristics 2 (V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------------------------|--|------------------------------|------|------------------------------|------|
| | | Min. | Typ. | Max. | |
| t _{wH} (SCLK1) | Serial I/O1 clock output "H" pulse width | t _c (SCLK1)/2-50 | | | ns |
| t _{wL} (SCLK1) | Serial I/O1 clock output "L" pulse width | t _c (SCLK1)/2-50 | | | ns |
| t _d (SCLK1-TxD) | Serial I/O1 output delay time (Note 1) | | | 350 | ns |
| t _v (SCLK1-TxD) | Serial I/O1 output valid time (Note 1) | -30 | | | ns |
| t _r (SCLK1) | Serial I/O1 clock output rising time | | | 50 | ns |
| t _f (SCLK1) | Serial I/O1 clock output falling time | | | 50 | ns |
| t _{wH} (SCLK2) | Serial I/O2 clock output "H" pulse width | t _c (SCLK2)/2-240 | | | ns |
| t _{wL} (SCLK2) | Serial I/O2 clock output "L" pulse width | t _c (SCLK2)/2-240 | | | ns |
| t _d (SCLK2-SOUT2) | Serial I/O2 output delay time | | | 0.2 X t _c (SCLK2) | ns |
| t _v (SCLK2-SOUT2) | Serial I/O2 output valid time | 0 | | | ns |
| t _f (SCLK2) | Serial I/O2 clock output falling time | | | 50 | ns |
| t _r (CMOS) | CMOS output rising time (Note 2) | | 20 | 50 | ns |
| t _f (CMOS) | CMOS output falling time (Note 2) | | 20 | 50 | ns |

Notes1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".
2: XOUT and XCOU pins are excluded.

**ELECTRICAL CHARACTERISTICS (EPROM or One Time PROM version)
ABSOLUTE MAXIMUM RATINGS (EPROM or One Time PROM version)**

Table 30 Absolute maximum ratings (EPROM or One Time PROM version)

| Symbol | Parameter | Conditions | Ratings | Unit | |
|--------|--|---|-------------------|-------------|---|
| VCC | Power source voltage | | -0.3 to 7.0 | V | |
| Vi | Input voltage P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67 | All voltages are based on Vss. Output transistors are cut off. | -0.3 to Vcc +0.3 | V | |
| Vi | Input voltage P70-P77 | | -0.3 to Vcc +0.3 | V | |
| Vi | Input voltage VL1 | | -0.3 to VL2 | V | |
| Vi | Input voltage VL2 | | VL1 to VL3 | V | |
| Vi | Input voltage VL3 | | VL2 to 7.0 | V | |
| Vi | Input voltage C1, C2 | | -0.3 to 7.0 | V | |
| Vi | Input voltage RESET, XIN | | -0.3 to Vcc +0.3 | V | |
| Vo | Output voltage C1, C2 | | -0.3 to 7.0 | V | |
| Vo | Output voltage P00-P07, P10-P15, P30-P37 | | At output port | -0.3 to Vcc | V |
| | | | At segment output | -0.3 to VL3 | V |
| Vo | Output voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77 | | -0.3 to Vcc +0.3 | V | |
| Vo | Output voltage VL3 | | -0.3 to 7.0 | V | |
| Vo | Output voltage VL2, SEG0-SEG17 | | -0.3 to VL3 | V | |
| Vo | Output voltage XOUT | | -0.3 to Vcc +0.3 | V | |
| Pd | Power dissipation | Ta = 25°C | 300 | mW | |
| Topr | Operating temperature | | -20 to 85 | °C | |
| Tstg | Storage temperature | | -40 to 125 | °C | |

RECOMMENDED OPERATING CONDITIONS (EPROM or One Time PROM version)

Table 31 Recommended operating conditions (1) (EPROM or One Time PROM version)
(Vcc = 2.5 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|--------|---------------------------------------|---|---------|------|---------|------|
| | | | Min. | Typ. | Max. | |
| VCC | Power source voltage | High-speed mode f(XIN) = 8 MHz | 4.0 | 5.0 | 5.5 | V |
| | | Middle-speed mode f(XIN) = 8 MHz | 2.5 | 5.0 | 5.5 | |
| | | Low-speed mode | 2.5 | 5.0 | 5.5 | |
| VSS | Power source voltage | | | 0 | | V |
| VREF | A-D, D-A conversion reference voltage | | 2.0 | | Vcc | V |
| AVSS | Analog power source voltage | | | 0 | | V |
| VIA | Analog input voltage AN0-AN7 | | AVSS | | Vcc | V |
| VIH | "H" input voltage | P00-P07, P10-P17, P40, P43, P45, P47, P50-P53, P56, P61, P64-P67, P71-P77 | 0.7 Vcc | | Vcc | V |
| VIH | "H" input voltage | P20-P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70 | 0.8 Vcc | | Vcc | V |
| VIH | "H" input voltage | RESET | 0.8 Vcc | | Vcc | V |
| VIH | "H" input voltage | XIN | 0.8 Vcc | | Vcc | V |
| VIL | "L" input voltage | P00-P07, P10-P17, P40, P43, P45, P47, P50-P53, P56, P61, P64-P67, P71-P77 | 0 | | 0.3 Vcc | V |
| VIL | "L" input voltage | P20-P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70 | 0 | | 0.2 Vcc | V |
| VIL | "L" input voltage | RESET | 0 | | 0.2 Vcc | V |
| VIL | "L" input voltage | XIN | 0 | | 0.2 Vcc | V |

Table 32 Recommended operating conditions (2) (EPROM or One Time PROM version)
(V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| ΣIOH(peak) | "H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | -20 | mA |
| ΣIOH(peak) | "H" total peak output current P41-P47, P50-P57, P60-P67 (Note 1) | | | -20 | mA |
| ΣIOL(peak) | "L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | 20 | mA |
| ΣIOL(peak) | "L" total peak output current P41-P47, P50-P57, P60-P67 (Note 1) | | | 20 | mA |
| ΣIOL(peak) | "L" total peak output current P40, P71-P77 (Note 1) | | | 80 | mA |
| ΣIOH(avg) | "H" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | -10 | mA |
| ΣIOH(avg) | "H" total average output current P41-P47, P50-P57, P60-P67 (Note 1) | | | -10 | mA |
| ΣIOL(avg) | "L" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | 10 | mA |
| ΣIOL(avg) | "L" total average output current P41-P47, P50-P57, P60-P67 (Note 1) | | | 10 | mA |
| ΣIOL(avg) | "L" total average output current P40, P71-P77 (Note 1) | | | 40 | mA |
| IOH(peak) | "H" peak output current P00-P07, P10-P15, P30-P37 (Note 2) | | | -1.0 | mA |
| IOH(peak) | "H" peak output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 2) | | | -5.0 | mA |
| IOL(peak) | "L" peak output current P00-P07, P10-P15, P30-P37 (Note 2) | | | 5.0 | mA |
| IOL(peak) | "L" peak output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 2) | | | 10 | mA |
| IOL(peak) | "L" peak output current P40, P71-P77 (Note 2) | | | 20 | mA |
| IOH(avg) | "H" average output current P00-P07, P10-P15, P30-P37 (Note 3) | | | -0.5 | mA |
| IOH(avg) | "H" average output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 3) | | | -2.5 | mA |
| IOL(avg) | "L" average output current P00-P07, P10-P15, P30-P37 (Note 3) | | | 2.5 | mA |
| IOL(avg) | "L" average output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 3) | | | 5.0 | mA |
| IOL(avg) | "L" average output current P40, P71-P77 (Note 3) | | | 10 | mA |

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

Table 33 Recommended operating conditions (3) (EPROM or One Time PROM version)
(V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------------|--|--|--------|------|----------------------------|------|
| | | | Min. | Typ. | Max. | |
| f(CNTR0) f(CNTR1) | Input frequency for timers X and Y (duty cycle 50%) | (4.0 V ≤ V _{CC} ≤ 5.5 V) | | | 4.0 | MHz |
| | | (V _{CC} ≤ 4.0 V) | | | (2×V _{CC}) -4 | MHz |
| f(XIN) | Main clock input oscillation frequency (Note 1) | High-speed mode (4.0 V ≤ V _{CC} ≤ 5.5 V) | | | 8.0 | MHz |
| | | High-speed mode (2.5 V ≤ V _{CC} ≤ 4.0 V) | | | (4×V _{CC}) -8 | MHz |
| | | Middle-speed mode | | | 8.0 | MHz |
| f(XCIN) | Sub-clock input oscillation frequency (Notes 1, 2) | | 32.768 | 50 | kHz | |

Notes 1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

ELECTRICAL CHARACTERISTICS (EPROM or One Time PROM version)

Table 34 Electrical characteristics (1) (EPROM or One Time PROM version)
 (VCC =4.0 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------|---|--|---------|--------|--------|------|
| | | | Min. | Typ. | Max. | |
| VOH | "H" output voltage P00-P07, P10-P15, P30-P37 | IOH = -1 mA | VCC-2.0 | | | V |
| | | IOH = -0.25 mA VCC = 2.5 V | VCC-0.8 | | | V |
| VOH | "H" output voltage P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 1) | IOH = -5 mA | VCC-2.0 | | | V |
| | | IOH = -1.5 mA | VCC-0.5 | | | V |
| | | IOH = -1.25 mA VCC = 2.5 V | VCC-0.8 | | | V |
| VOL | "L" output voltage P00-P07, P10-P15, P30-P37 | IOL = 5 mA | | | 2.0 | V |
| | | IOL = 1.5 mA | | | 0.5 | V |
| | | IOL = 1.25 mA VCC = 2.5 V | | | 0.8 | V |
| VOL | "L" output voltage P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 | IOL = 10 mA | | | 2.0 | V |
| | | IOL = 3.0 mA | | | 0.5 | V |
| | | IOL = 2.5 mA VCC = 2.5 V | | | 0.8 | V |
| VOL | "L" output voltage P40, P71-P77 | IOL = 10 mA | | | 0.5 | V |
| | | IOL = 5 mA VCC = 2.5 V | | | 0.3 | V |
| VT+ - VT- | Hysteresis INT0-INT2, ADT, CNTR0, CNTR1, P20-P27 | | | 0.5 | | V |
| VT+ - VT- | Hysteresis SCLK, RxD, SIN2 | | | 0.5 | | V |
| VT+ - VT- | Hysteresis RESET | | | 0.5 | | V |
| IiH | "H" input current P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67, P70-P77 | Vi = VCC | | | 5.0 | μA |
| IiH | "H" input current RESET | Vi = VCC | | | 5.0 | μA |
| IiH | "H" input current XIN | Vi = VCC | | 4.0 | | μA |
| IiL | "L" input current P00-P07, P10-P17, P20-P27, P41-P47, P50-P57, P60-P67 | Vi = VSS Pull-ups "off" | | | -5.0 | μA |
| | | VCC = 5 V, Vi = VSS Pull-ups "on" | -60.0 | -120.0 | -240.0 | μA |
| | | VCC = 2.5 V, Vi = VSS Pull-ups "on" | -6.0 | -25.0 | -45.0 | μA |
| IiL | "L" input current P40, P70-P77 | | | | -5.0 | μA |
| IiL | "L" input current RESET | Vi = VSS | | | -5.0 | μA |
| IiL | "L" input current XIN | Vi = VSS | | -4.0 | | μA |
| ILOAD | Output load current P30-P37 | VCC = 5.0 V, Vo = VCC, Pullup ON Output transistors "off" | -60.0 | -120.0 | -240.0 | μA |
| | | VCC = 2.5 V, Vo = VCC, Pullup ON Output transistors "off" | -6.0 | -25.0 | -45.0 | μA |
| ILEAK | Output leak current P30-P37 | Vo = VCC, Pullup OFF Output transistors "off" | | | 5.0 | μA |
| | | Vo = VSS, Pullup OFF Output transistors "off" | | | -5.0 | μA |

Table 35 Electrical characteristics (2) (EPROM or One Time PROM version)
(V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|--------|---|--|--|------|------|------|
| | | | Min. | Typ. | Max. | |
| VRAM | RAM retention voltage | At clock stop mode | 2.0 | | 5.5 | V |
| ICC | Power source current | <ul style="list-style-type: none"> High-speed mode, V_{CC} = 5 V f(X_{IN}) = 8 MHz f(X_{CIN}) = 32.768 kHz Output transistors "off" A-D converter in operating | | 6.4 | 13 | mA |
| | | <ul style="list-style-type: none"> High-speed mode, V_{CC} = 5 V f(X_{IN}) = 8 MHz (in WIT state) f(X_{CIN}) = 32.768 kHz Output transistors "off" A-D converter stop | | 1.6 | 3.2 | mA |
| | | <ul style="list-style-type: none"> Low-speed mode, V_{CC} = 5 V, T_a ≤ 55°C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz Output transistors "off" | | 35 | 70 | μA |
| | | <ul style="list-style-type: none"> Low-speed mode, V_{CC} = 5 V, T_a = 25°C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz (in WIT state) Output transistors "off" | | 20 | 40 | μA |
| | | <ul style="list-style-type: none"> Low-speed mode, V_{CC} = 3 V, T_a ≤ 55°C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz Output transistors "off" | | 15 | 22 | μA |
| | | <ul style="list-style-type: none"> Low-speed mode, V_{CC} = 3 V, T_a = 25°C f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz (in WIT state) Output transistors "off" | | 4.5 | 9.0 | μA |
| | | All oscillation stopped (in STP state) Output transistors "off" | T _a = 25 °C T _a = 85 °C | 0.1 | 1.0 | 10 |
| VL1 | Power source voltage | When using voltage multiplier | 1.3 | 1.8 | 2.3 | V |
| IL1 | Power source current (VL1) (Note) | VL1 = 1.8 V | | 4.0 | | μA |

Note: When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".

A-D CONVERTER CHARACTERISTICS (EPROM or One Time PROM version)

Table 36 A-D converter characteristics (EPROM or One Time PROM version)

(VCC = 2.7 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85°C, f(XIN) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)
 8-bit A-D mode (when conversion mode selection bit (bit 0 of address 001416) is "1")

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------|--|---------------------------|--------|------|------|---------------------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute accuracy (excluding quantization error) | VCC = VREF = 2.7 to 5.5 V | | | ±2 | LSB |
| tCONV | Conversion time | | 49 | | 50 | tc(ADCLK) (Note) |
| RLADDER | Ladder resistor | | 12 | 35 | 100 | kΩ |
| IVREF | Reference power source input current | VREF = 5 V | 50 | 150 | 200 | μA |
| I _{IA} | Analog port input current | | | | 5.0 | μA |

Note: ADCLK is the control clock of the A-D converter. System clock φ is used.

Table 37 A-D converter characteristics (EPROM or One Time PROM version)

(VCC = 2.7 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85°C, f(XIN) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)
 10-bit A-D mode (when conversion mode selection bit (bit 0 of address 001416) is "0")

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------|--|---------------------------|--------|------|------|---------------------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 10 | Bits |
| – | Absolute accuracy (excluding quantization error) | VCC = VREF = 2.7 to 5.5 V | | | ±4 | LSB |
| tCONV | Conversion time | | 61 | | 62 | tc(ADCLK) (Note) |
| RLADDER | Ladder resistor | | 12 | 35 | 100 | kΩ |
| IVREF | Reference power source input current | VREF = 5 V | 50 | 150 | 200 | μA |
| I _{IA} | Analog port input current | | | | 5.0 | μA |

Note: ADCLK is the control clock of the A-D converter. System clock φ is used.

D-A CONVERTER CHARACTERISTICS (EPROM or One Time PROM version)

Table 38 D-A converter characteristics (EPROM or One Time PROM version)

(VCC = 2.7 to 5.5 V, VCC = VREF, VSS = AVSS = 0 V, Ta = -20 to 85°C, in middle/high-speed mode unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|--------|--------------------------------------|--------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute accuracy | VCC = VREF = 5 V | | | 1.0 | % |
| | | VCC = VREF = 2.7 V | | | 2.0 | % |
| tsu | Setting time | | | 3 | | μs |
| RO | Output resistor | | 1 | 2.5 | 4 | kΩ |
| IVREF | Reference power source input current | (Note) | | | 3.2 | mA |

Note: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.

TIMING REQUIREMENTS (EPROM or One Time PROM version)

Table 39 Timing requirements 1 (EPROM or One Time PROM version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _w (RESET) | Reset input "L" pulse width | 2 | | | μs |
| t _c (X _{IN}) | Main clock input cycle time (X _{IN} input) | 125 | | | ns |
| t _{wH} (X _{IN}) | Main clock input "H" pulse width | 45 | | | ns |
| t _{wL} (X _{IN}) | Main clock input "L" pulse width | 40 | | | ns |
| t _c (CNTR) | CNTR ₀ , CNTR ₁ input cycle time | 250 | | | ns |
| t _{wH} (CNTR) | CNTR ₀ , CNTR ₁ input "H" pulse width | 105 | | | ns |
| t _{wL} (CNTR) | CNTR ₀ , CNTR ₁ input "L" pulse width | 105 | | | ns |
| t _{wH} (INT) | INT ₀ to INT ₂ input "H" pulse width | 80 | | | ns |
| t _{wL} (INT) | INT ₀ to INT ₂ input "L" pulse width | 80 | | | ns |
| t _c (SCLK1) | Serial I/O1 clock input cycle time (Note) | 800 | | | ns |
| t _{wH} (SCLK1) | Serial I/O1 clock input "H" pulse width (Note) | 370 | | | ns |
| t _{wL} (SCLK1) | Serial I/O1 clock input "L" pulse width (Note) | 370 | | | ns |
| t _{su} (RxD-SCLK1) | Serial I/O1 input set up time | 220 | | | ns |
| t _h (SCLK1-RxD) | Serial I/O1 input hold time | 100 | | | ns |
| t _c (SCLK2) | Serial I/O2 clock input cycle time (Note) | 1000 | | | ns |
| t _{wH} (SCLK2) | Serial I/O2 clock input "H" pulse width (Note) | 400 | | | ns |
| t _{wL} (SCLK2) | Serial I/O2 clock input "L" pulse width (Note) | 400 | | | ns |
| t _{su} (S _{IN2} -SCLK2) | Serial I/O2 input set up time | 200 | | | ns |
| t _h (SCLK2-S _{IN2}) | Serial I/O2 input hold time | 200 | | | ns |

Note: When bit 6 of address 001A₁₆ is "1".

Divide this value by four when bit 6 of address 001A₁₆ is "0".

Table 40 Timing requirements 2 (EPROM or One Time PROM version)

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|-----------------------------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _w (RESET) | Reset input "L" pulse width | 2 | | | μs |
| t _c (X _{IN}) | Main clock input cycle time (X _{IN} input) | 125 | | | ns |
| t _{wH} (X _{IN}) | Main clock input "H" pulse width | 45 | | | ns |
| t _{wL} (X _{IN}) | Main clock input "L" pulse width | 40 | | | ns |
| t _c (CNTR) | CNTR ₀ , CNTR ₁ input cycle time | 500/(V _{CC} -2) | | | ns |
| t _{wH} (CNTR) | CNTR ₀ , CNTR ₁ input "H" pulse width | 250/(V _{CC} -2)-20 | | | ns |
| t _{wL} (CNTR) | CNTR ₀ , CNTR ₁ input "L" pulse width | 250/(V _{CC} -2)-20 | | | ns |
| t _{wH} (INT) | INT ₀ to INT ₂ input "H" pulse width | 230 | | | ns |
| t _{wL} (INT) | INT ₀ to INT ₂ input "L" pulse width | 230 | | | ns |
| t _c (SCLK1) | Serial I/O1 clock input cycle time (Note) | 2000 | | | ns |
| t _{wH} (SCLK1) | Serial I/O1 clock input "H" pulse width (Note) | 950 | | | ns |
| t _{wL} (SCLK1) | Serial I/O1 clock input "L" pulse width (Note) | 950 | | | ns |
| t _{su} (RxD-SCLK1) | Serial I/O1 input set up time | 400 | | | ns |
| t _h (SCLK1-RxD) | Serial I/O1 input hold time | 200 | | | ns |
| t _c (SCLK2) | Serial I/O2 clock input cycle time (Note) | 2000 | | | ns |
| t _{wH} (SCLK2) | Serial I/O2 clock input "H" pulse width (Note) | 950 | | | ns |
| t _{wL} (SCLK2) | Serial I/O2 clock input "L" pulse width (Note) | 950 | | | ns |
| t _{su} (S _{IN2} -SCLK2) | Serial I/O2 input set up time | 400 | | | ns |
| t _h (SCLK2-S _{IN2}) | Serial I/O2 input hold time | 300 | | | ns |

Note: When bit 6 of address 001A₁₆ is "1".

Divide this value by four when bit 6 of address 001A₁₆ is "0".

SWITCHING CHARACTERISTICS (EPROM or One Time PROM version)**Table 41 Switching characteristics 1 (EPROM or One Time PROM version)**(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------------------------|--|------------------------------|------|------------------------------|------|
| | | Min. | Typ. | Max. | |
| t _{wH} (SCLK1) | Serial I/O1 clock output "H" pulse width | t _c (SCLK1)/2-30 | | | ns |
| t _{wL} (SCLK1) | Serial I/O1 clock output "L" pulse width | t _c (SCLK1)/2-30 | | | ns |
| t _d (SCLK1-TxD) | Serial I/O1 output delay time (Note 1) | | | 140 | ns |
| t _v (SCLK1-TxD) | Serial I/O1 output valid time (Note 1) | -30 | | | ns |
| t _r (SCLK1) | Serial I/O1 clock output rising time | | | 30 | ns |
| t _f (SCLK1) | Serial I/O1 clock output falling time | | | 30 | ns |
| t _{wH} (SCLK2) | Serial I/O2 clock output "H" pulse width | t _c (SCLK2)/2-160 | | | ns |
| t _{wL} (SCLK2) | Serial I/O2 clock output "L" pulse width | t _c (SCLK2)/2-160 | | | ns |
| t _d (SCLK2-SOUT2) | Serial I/O2 output delay time | | | 0.2 X t _c (SCLK2) | ns |
| t _v (SCLK2-SOUT2) | Serial I/O2 output valid time | 0 | | | ns |
| t _f (SCLK2) | Serial I/O2 clock output falling time | | | 40 | ns |
| t _r (CMOS) | CMOS output rising time (Note 2) | | 10 | 30 | ns |
| t _f (CMOS) | CMOS output falling time (Note 2) | | 10 | 30 | ns |

Notes1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".**2:** XOUT and XCOUNT pins are excluded.**Table 42 Switching characteristics 2 (EPROM or One Time PROM version)**(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------------------------|--|------------------------------|------|------------------------------|------|
| | | Min. | Typ. | Max. | |
| t _{wH} (SCLK1) | Serial I/O1 clock output "H" pulse width | t _c (SCLK1)/2-50 | | | ns |
| t _{wL} (SCLK1) | Serial I/O1 clock output "L" pulse width | t _c (SCLK1)/2-50 | | | ns |
| t _d (SCLK1-TxD) | Serial I/O1 output delay time (Note 1) | | | 350 | ns |
| t _v (SCLK1-TxD) | Serial I/O1 output valid time (Note 1) | -30 | | | ns |
| t _r (SCLK1) | Serial I/O1 clock output rising time | | | 50 | ns |
| t _f (SCLK1) | Serial I/O1 clock output falling time | | | 50 | ns |
| t _{wH} (SCLK2) | Serial I/O2 clock output "H" pulse width | t _c (SCLK2)/2-240 | | | ns |
| t _{wL} (SCLK2) | Serial I/O2 clock output "L" pulse width | t _c (SCLK2)/2-240 | | | ns |
| t _d (SCLK2-SOUT2) | Serial I/O2 output delay time | | | 0.2 X t _c (SCLK2) | ns |
| t _v (SCLK2-SOUT2) | Serial I/O2 output valid time | 0 | | | ns |
| t _f (SCLK2) | Serial I/O2 clock output falling time | | | 50 | ns |
| t _r (CMOS) | CMOS output rising time (Note 2) | | 20 | 50 | ns |
| t _f (CMOS) | CMOS output falling time (Note 2) | | 20 | 50 | ns |

Notes1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".**2:** XOUT and XCOUNT pins are excluded.

ELECTRICAL CHARACTERISTICS (Extended operating temperature version)
ABSOLUTE MAXIMUM RATINGS (Extended operating temperature version)

Table 43 Absolute maximum ratings (Extended operating temperature version)

| Symbol | Parameter | Conditions | Ratings | Unit | |
|--------|--|---|-------------------|-------------|---|
| VCC | Power source voltage (Note 1) | All voltages are based on Vss. Output transistors are cut off. | -0.3 to 6.5 | V | |
| Vi | Input voltage P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67 | | -0.3 to Vcc +0.3 | V | |
| Vi | Input voltage P70-P77 | | -0.3 to Vcc +0.3 | V | |
| Vi | Input voltage VL1 | | -0.3 to VL2 | V | |
| Vi | Input voltage VL2 | | VL1 to VL3 | V | |
| Vi | Input voltage VL3 (Note 2) | | VL2 to 6.5 | V | |
| Vi | Input voltage C1, C2 (Note 1) | | -0.3 to 6.5 | V | |
| Vi | Input voltage RESET, XIN | | -0.3 to Vcc +0.3 | V | |
| Vo | Output voltage C1, C2 (Note 1) | | -0.3 to 6.5 | V | |
| Vo | Output voltage P00-P07, P10-P15, P30-P37 | | At output port | -0.3 to Vcc | V |
| | | | At segment output | -0.3 to VL3 | V |
| Vo | Output voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77 | | -0.3 to Vcc +0.3 | V | |
| Vo | Output voltage VL3 (Note 1) | | -0.3 to 6.5 | V | |
| Vo | Output voltage VL2, SEG0-SEG17 | -0.3 to VL3 | V | | |
| Vo | Output voltage XOUT | -0.3 to Vcc +0.3 | V | | |
| Pd | Power dissipation | Ta = 25°C | 300 | mW | |
| Topr | Operating temperature | | -40 to 85 | °C | |
| Tstg | Storage temperature | | -65 to 150 | °C | |

Notes 1: -0.3 V to 7.0 V for M37560EFD.

2: VL2 to 7.0 V for M37560EFD

RECOMMENDED OPERATING CONDITIONS (Extended operating temperature version)

Table 44 Recommended operating conditions (1) (Extended operating temperature version)

(Vcc = 2.5 to 5.5 V, Ta = -20 to 85°C, and Vcc = 3.0 to 5.5 V, Ta = -40 to -20 °C unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit | |
|--------|---------------------------------------|---|--------------------|------|---------|------|-----|
| | | | Min. | Typ. | Max. | | |
| VCC | Power source voltage | High-speed mode f(XIN) = 8 MHz | 4.0 | 5.0 | 5.5 | V | |
| | | Middle-speed mode f(XIN) = 8 MHz | Ta = -20 to 85 °C | 2.5 | 5.0 | | 5.5 |
| | | | Ta = -40 to -20 °C | 3.0 | 5.0 | | 5.5 |
| | | Low-speed mode | Ta = -20 to 85 °C | 2.5 | 5.0 | | 5.5 |
| | | | Ta = -40 to -20 °C | 3.0 | 5.0 | | 5.5 |
| VSS | Power source voltage | | | 0 | | V | |
| VREF | A-D, D-A conversion reference voltage | | 2.0 | | Vcc | V | |
| AVSS | Analog power source voltage | | | 0 | | V | |
| VIA | Analog input voltage AN0-AN7 | | AVSS | | Vcc | V | |
| VIH | "H" input voltage | P00-P07, P10-P17, P40, P43, P45, P47, P50-P53, P56, P61, P64-P67, P71-P77 | 0.7 Vcc | | Vcc | V | |
| VIH | "H" input voltage | P20-P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70 | 0.8 Vcc | | Vcc | V | |
| VIH | "H" input voltage | RESET | 0.8 Vcc | | Vcc | V | |
| VIH | "H" input voltage | XIN | 0.8 Vcc | | Vcc | V | |
| VIL | "L" input voltage | P00-P07, P10-P17, P40, P43, P45, P47, P50-P53, P56, P61, P64-P67, P71-P77 | 0 | | 0.3 Vcc | V | |
| VIL | "L" input voltage | P20-P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70 | 0 | | 0.2 Vcc | V | |
| VIL | "L" input voltage | RESET | 0 | | 0.2 Vcc | V | |
| VIL | "L" input voltage | XIN | 0 | | 0.2 Vcc | V | |

Table 45 Recommended operating conditions (2) (Extended operating temperature version)
 (V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, and V_{CC} = 3.0 to 5.5 V, T_a = -40 to -20 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------|--|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| ΣIOH(peak) | "H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | -20 | mA |
| ΣIOH(peak) | "H" total peak output current P41-P47, P50-P57, P60-P67 (Note 1) | | | -20 | mA |
| ΣIOL(peak) | "L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | 20 | mA |
| ΣIOL(peak) | "L" total peak output current P41-P47, P50-P57, P60-P67 (Note 1) | | | 20 | mA |
| ΣIOL(peak) | "L" total peak output current P40, P71-P77 (Note 1) | | | 80 | mA |
| ΣIOH(avg) | "H" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | -10 | mA |
| ΣIOH(avg) | "H" total average output current P41-P47, P50-P57, P60-P67 (Note 1) | | | -10 | mA |
| ΣIOL(avg) | "L" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1) | | | 10 | mA |
| ΣIOL(avg) | "L" total average output current P41-P47, P50-P57, P60-P67 (Note 1) | | | 10 | mA |
| ΣIOL(avg) | "L" total average output current P40, P71-P77 (Note 1) | | | 40 | mA |
| IOH(peak) | "H" peak output current P00-P07, P10-P15, P30-P37 (Note 2) | | | -1.0 | mA |
| IOH(peak) | "H" peak output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 2) | | | -5.0 | mA |
| IOL(peak) | "L" peak output current P00-P07, P10-P15, P30-P37 (Note 2) | | | 5.0 | mA |
| IOL(peak) | "L" peak output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 2) | | | 10 | mA |
| IOL(peak) | "L" peak output current P40, P71-P77 (Note 2) | | | 20 | mA |
| IOH(avg) | "H" average output current P00-P07, P10-P15, P30-P37 (Note 3) | | | -0.5 | mA |
| IOH(avg) | "H" average output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 3) | | | -2.5 | mA |
| IOL(avg) | "L" average output current P00-P07, P10-P15, P30-P37 (Note 3) | | | 2.5 | mA |
| IOL(avg) | "L" average output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 3) | | | 5.0 | mA |
| IOL(avg) | "L" average output current P40, P71-P77 (Note 3) | | | 10 | mA |

Notes1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

Table 46 Recommended operating conditions (3) (Extended operating temperature version)
 (V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, and V_{CC} = 3.0 to 5.5 V, T_a = -40 to -20 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------------|---|---|--------|------|----------------------------|------|
| | | | Min. | Typ. | Max. | |
| f(CNTR0) f(CNTR1) | Input frequency for timers X and Y (duty cycle 50%) | (4.0 V ≤ V _{CC} ≤ 5.5 V) | | | 4.0 | MHz |
| | | (V _{CC} ≤ 4.0 V) | | | (2×V _{CC}) -4 | MHz |
| f(XIN) | Main clock input oscillation frequency (Note 1) | High-speed mode (4.0 V ≤ V _{CC} ≤ 5.5 V) | | | 8.0 | MHz |
| | | High-speed mode (V _{CC} ≤ 4.0 V) | | | (4×V _{CC}) -8 | MHz |
| | | Middle-speed mode | | | 8.0 | MHz |
| f(XCIN) | Sub-clock input oscillation frequency (Notes 1, 2) | | 32.768 | 50 | kHz | |

Notes1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

ELECTRICAL CHARACTERISTICS (Extended operating temperature version)

Table 47 Electrical characteristics (1) (V_{CC} =4.0 to 5.5 V, T_a = -40 to 85°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------------------------|---|---|----------------------|--------|--------|------|
| | | | Min. | Typ. | Max. | |
| V _{OH} | "H" output voltage P00-P07, P10-P15, P30-P37 | I _{OH} = -1 mA | V _{CC} -2.0 | | | V |
| | | I _{OH} = -0.25 mA V _{CC} = 3.0 V | V _{CC} -1.0 | | | V |
| V _{OH} | "H" output voltage P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 1) | I _{OH} = -5 mA | V _{CC} -2.0 | | | V |
| | | I _{OH} = -1.5 mA | V _{CC} -0.5 | | | V |
| | | I _{OH} = -1.25 mA V _{CC} = 3.0 V | V _{CC} -1.0 | | | V |
| V _{OL} | "L" output voltage P00-P07, P10-P15, P30-P37 | I _{OL} = 5 mA | | | 2.0 | V |
| | | I _{OL} = 1.5 mA | | | 0.5 | V |
| | | I _{OL} = 1.25 mA V _{CC} = 3.0 V | | | 1.0 | V |
| V _{OL} | "L" output voltage P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 | I _{OL} = 10 mA | | | 2.0 | V |
| | | I _{OL} = 3.0 mA | | | 0.5 | V |
| | | I _{OL} = 3.0 mA V _{CC} = 3.0 V | | | 1.0 | V |
| V _{OL} | "L" output voltage P40, P71-P77 | I _{OL} = 10 mA | | | 0.5 | V |
| | | I _{OL} = 5 mA V _{CC} = 3.0 V | | | 0.4 | V |
| V _{T+} - V _{T-} | Hysteresis INT0-INT2, ADT, CNTR0, CNTR1, P20-P27 | | | 0.5 | | V |
| V _{T+} - V _{T-} | Hysteresis SCLK, RxD, SIN2 | | | 0.5 | | V |
| V _{T+} - V _{T-} | Hysteresis RESET | | | 0.5 | | V |
| I _{IH} | "H" input current P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67, P70-P77 | V _I = V _{CC} | | | 5.0 | μA |
| I _{IH} | "H" input current RESET | V _I = V _{CC} | | | 5.0 | μA |
| I _{IH} | "H" input current XIN | V _I = V _{CC} | | 4.0 | | μA |
| I _{IL} | "L" input current P00-P07, P10-P17, P20-P27, P41-P47, P50-P57, P60-P67 | V _I = V _{SS} Pull-ups "off" | | | -5.0 | μA |
| | | V _{CC} = 5 V, V _I = V _{SS} Pull-ups "on" | -60.0 | -120.0 | -240.0 | μA |
| | | V _{CC} = 3.0 V, V _I = V _{SS} Pull-ups "on" | -7.0 | -30.0 | -55.0 | μA |
| I _{IL} | "L" input current P40, P70-P77 | | | | -5.0 | μA |
| I _{IL} | "L" input current RESET | V _I = V _{SS} | | | -5.0 | μA |
| I _{IL} | "L" input current XIN | V _I = V _{SS} | | -4.0 | | μA |
| I _{LOAD} | Output load current P30-P37 | V _{CC} = 5.0 V, V _O = V _{CC} , Pullup ON Output transistors "off" | -60.0 | -120.0 | -240.0 | μA |
| | | V _{CC} = 3.0 V, V _O = V _{CC} , Pullup ON Output transistors "off" | -7.0 | -30.0 | -55.0 | μA |
| I _{LEAK} | Output leak current P30-P37 | V _O = V _{CC} , Pullup OFF Output transistors "off" | | | 5.0 | μA |
| | | V _O = V _{SS} , Pullup OFF Output transistors "off" | | | -5.0 | μA |

Table 48 Electrical characteristics (2) (Extended operating temperature version)
 (VCC = 2.5 to 5.5 V, Ta = -20 to 85°C, and VCC = 3.0 to 5.5 V, Ta = -40 to -20°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit | |
|--------|---|---|--------------------------|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| VRAM | RAM retention voltage | At clock stop mode | 2.0 | | 5.5 | V | |
| ICC | Power source current | <ul style="list-style-type: none"> High-speed mode, VCC = 5 V f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors "off" A-D converter in operating | | 6.4 | 13 | mA | |
| | | <ul style="list-style-type: none"> High-speed mode, VCC = 5 V f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors "off" A-D converter stop | | 1.6 | 3.2 | mA | |
| | | <ul style="list-style-type: none"> Low-speed mode, VCC = 5 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off" | | 35 | 70 | μA | |
| | | <ul style="list-style-type: none"> Low-speed mode, VCC = 5 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off" | | 20 | 40 | μA | |
| | | <ul style="list-style-type: none"> Low-speed mode, VCC = 3 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off" | | 15 | 22 | μA | |
| | | <ul style="list-style-type: none"> Low-speed mode, VCC = 3 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off" | | 4.5 | 9.0 | μA | |
| | | All oscillation stopped (in STP state) Output transistors "off" | Ta = 25 °C Ta = 85 °C | | 0.1 | 10 | μA |
| VL1 | Power source voltage | When using voltage multiplier | M37560MFD | 1.3 | 1.8 | 2.1 | V |
| | | | M37560EFD | 1.3 | 1.8 | 2.3 | |
| IL1 | Power source current (VL1) (Note) | VL1 = 1.8 V | | 4.0 | | μA | |

Note: When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".

A-D CONVERTER CHARACTERISTICS (Extended operating temperature version)

Table 49 A-D converter characteristics (Extended operating temperature version)

(VCC = 3.0 to 5.5 V, VSS = AVSS = 0 V, Ta = -40 to 85°C, f(XIN) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)
 8-bit A-D mode (when conversion mode selection bit (bit 0 of address 001416) is "1")

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------|--|---------------------------|--------|------|------|---------------------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute accuracy (excluding quantization error) | VCC = VREF = 3.0 to 5.5 V | | | ±2 | LSB |
| tCONV | Conversion time | | 49 | | 50 | tc(ADCLK) (Note) |
| RLADDER | Ladder resistor | | 12 | 35 | 100 | kΩ |
| IVREF | Reference power source input current | VREF = 5 V | 50 | 150 | 200 | μA |
| I _{IA} | Analog port input current | | | | 5.0 | μA |

Note: ADCLK is the control clock of the A-D converter. System clock φ is used.

Table 50 A-D converter characteristics (Extended operating temperature version)

(VCC = 3.0 to 5.5 V, VSS = AVSS = 0 V, Ta = -40 to 85°C, f(XIN) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)
 10-bit A-D mode (when conversion mode selection bit (bit 0 of address 001416) is "0")

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------|--|---------------------------|--------|------|------|---------------------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 10 | Bits |
| – | Absolute accuracy (excluding quantization error) | VCC = VREF = 3.0 to 5.5 V | | | ±4 | LSB |
| tCONV | Conversion time | | 61 | | 62 | tc(ADCLK) (Note) |
| RLADDER | Ladder resistor | | 12 | 35 | 100 | kΩ |
| IVREF | Reference power source input current | VREF = 5 V | 50 | 150 | 200 | μA |
| I _{IA} | Analog port input current | | | | 5.0 | μA |

Note: ADCLK is the control clock of the A-D converter. System clock φ is used.

D-A CONVERTER CHARACTERISTICS (Extended operating temperature version)

Table 51 D-A converter characteristics (Extended operating temperature version)

(VCC = 3.0 to 5.5 V, VCC = VREF, VSS = AVSS = 0 V, Ta = -40 to 85°C, in middle/high-speed mode unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------|--------------------------------------|--------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute accuracy | VCC = VREF = 5 V | | | 1.0 | % |
| | | VCC = VREF = 3.0 V | | | 2.0 | % |
| t _{su} | Setting time | | | 3 | μs | |
| RO | Output resistor | | 1 | 2.5 | 4 | kΩ |
| IVREF | Reference power source input current | (Note) | | | 3.2 | mA |

Note: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.

TIMING REQUIREMENTS (Extended operating temperature version)

Table 52 Timing requirements 1 (Extended operating temperature version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -40 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| tw(RESET) | Reset input "L" pulse width | 2 | | | μs |
| tc(XIN) | Main clock input cycle time (XIN input) | 125 | | | ns |
| twH(XIN) | Main clock input "H" pulse width | 45 | | | ns |
| twL(XIN) | Main clock input "L" pulse width | 40 | | | ns |
| tc(CNTR) | CNTR0, CNTR1 input cycle time | 250 | | | ns |
| twH(CNTR) | CNTR0, CNTR1 input "H" pulse width | 105 | | | ns |
| twL(CNTR) | CNTR0, CNTR1 input "L" pulse width | 105 | | | ns |
| twH(INT) | INT0 to INT2 input "H" pulse width | 80 | | | ns |
| twL(INT) | INT0 to INT2 input "L" pulse width | 80 | | | ns |
| tc(SCLK1) | Serial I/O1 clock input cycle time (Note) | 800 | | | ns |
| twH(SCLK1) | Serial I/O1 clock input "H" pulse width (Note) | 370 | | | ns |
| twL(SCLK1) | Serial I/O1 clock input "L" pulse width (Note) | 370 | | | ns |
| tsu(RxD-SCLK1) | Serial I/O1 input set up time | 220 | | | ns |
| th(SCLK1-RxD) | Serial I/O1 input hold time | 100 | | | ns |
| tc(SCLK2) | Serial I/O2 clock input cycle time (Note) | 1000 | | | ns |
| twH(SCLK2) | Serial I/O2 clock input "H" pulse width (Note) | 400 | | | ns |
| twL(SCLK2) | Serial I/O2 clock input "L" pulse width (Note) | 400 | | | ns |
| tsu(SIN2-SCLK2) | Serial I/O2 input set up time | 200 | | | ns |
| th(SCLK2-SIN2) | Serial I/O2 input hold time | 200 | | | ns |

Note: When bit 6 of address 001A16 is "1".

Divide this value by four when bit 6 of address 001A16 is "0".

Table 53 Timing requirements 2 (Extended operating temperature version)

(VCC = 2.5 to 4.0 V, VSS = 0 V, Ta = -20 to 85°C, and VCC = 3.0 to 5.5 V, Ta = -40 to -20°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------|---|----------------|------|------|------|
| | | Min. | Typ. | Max. | |
| tw(RESET) | Reset input "L" pulse width | 2 | | | μs |
| tc(XIN) | Main clock input cycle time (XIN input) | 125 | | | ns |
| twH(XIN) | Main clock input "H" pulse width | 45 | | | ns |
| twL(XIN) | Main clock input "L" pulse width | 40 | | | ns |
| tc(CNTR) | CNTR0, CNTR1 input cycle time | 500/(VCC-2) | | | ns |
| twH(CNTR) | CNTR0, CNTR1 input "H" pulse width | 250/(VCC-2)-20 | | | ns |
| twL(CNTR) | CNTR0, CNTR1 input "L" pulse width | 250/(VCC-2)-20 | | | ns |
| twH(INT) | INT0 to INT2 input "H" pulse width | 230 | | | ns |
| twL(INT) | INT0 to INT2 input "L" pulse width | 230 | | | ns |
| tc(SCLK1) | Serial I/O1 clock input cycle time (Note) | 2000 | | | ns |
| twH(SCLK1) | Serial I/O1 clock input "H" pulse width (Note) | 950 | | | ns |
| twL(SCLK1) | Serial I/O1 clock input "L" pulse width (Note) | 950 | | | ns |
| tsu(RxD-SCLK1) | Serial I/O1 input set up time | 400 | | | ns |
| th(SCLK1-RxD) | Serial I/O1 input hold time | 200 | | | ns |
| tc(SCLK2) | Serial I/O2 clock input cycle time (Note) | 2000 | | | ns |
| twH(SCLK2) | Serial I/O2 clock input "H" pulse width (Note) | 950 | | | ns |
| twL(SCLK2) | Serial I/O2 clock input "L" pulse width (Note) | 950 | | | ns |
| tsu(SIN2-SCLK2) | Serial I/O2 input set up time | 400 | | | ns |
| th(SCLK2-SIN2) | Serial I/O2 input hold time | 300 | | | ns |

Note: When bit 6 of address 001A16 is "1".

Divide this value by four when bit 6 of address 001A16 is "0".

SWITCHING CHARACTERISTICS (Extended operating temperature version)

Table 54 Switching characteristics 1 (Extended operating temperature version)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = -40 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------|--|------------------|------|------------------|------|
| | | Min. | Typ. | Max. | |
| twH(SCLK1) | Serial I/O1 clock output "H" pulse width | tc (SCLK1)/2-30 | | | ns |
| twL(SCLK1) | Serial I/O1 clock output "L" pulse width | tc (SCLK1)/2-30 | | | ns |
| td(SCLK1-TxD) | Serial I/O1 output delay time (Note 1) | | | 140 | ns |
| tv(SCLK1-TxD) | Serial I/O1 output valid time (Note 1) | -30 | | | ns |
| tr(SCLK1) | Serial I/O1 clock output rising time | | | 30 | ns |
| tf(SCLK1) | Serial I/O1 clock output falling time | | | 30 | ns |
| twH(SCLK2) | Serial I/O2 clock output "H" pulse width | tc (SCLK2)/2-160 | | | ns |
| twL(SCLK2) | Serial I/O2 clock output "L" pulse width | tc (SCLK2)/2-160 | | | ns |
| td(SCLK2-SOUT2) | Serial I/O2 output delay time | | | 0.2 X tc (SCLK2) | ns |
| tv(SCLK2-SOUT2) | Serial I/O2 output valid time | 0 | | | ns |
| tf(SCLK2) | Serial I/O2 clock output falling time | | | 40 | ns |
| tr(CMOS) | CMOS output rising time (Note 2) | | 10 | 30 | ns |
| tf(CMOS) | CMOS output falling time (Note 2) | | 10 | 30 | ns |

Notes1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2: XOUT and XCOUT pins are excluded.

Table 55 Switching characteristics 2 (Extended operating temperature version)

(Vcc = 2.5 to 4.0 V, Vss = 0 V, Ta = -20 to 85°C, and Vcc = 3.0 to 5.5 V, Ta = -40 to -20°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------|--|------------------|------|------------------|------|
| | | Min. | Typ. | Max. | |
| twH(SCLK1) | Serial I/O1 clock output "H" pulse width | tc (SCLK1)/2-50 | | | ns |
| twL(SCLK1) | Serial I/O1 clock output "L" pulse width | tc (SCLK1)/2-50 | | | ns |
| td(SCLK1-TxD) | Serial I/O1 output delay time (Note 1) | | | 350 | ns |
| tv(SCLK1-TxD) | Serial I/O1 output valid time (Note 1) | -30 | | | ns |
| tr(SCLK1) | Serial I/O1 clock output rising time | | | 50 | ns |
| tf(SCLK1) | Serial I/O1 clock output falling time | | | 50 | ns |
| twH(SCLK2) | Serial I/O2 clock output "H" pulse width | tc (SCLK2)/2-240 | | | ns |
| twL(SCLK2) | Serial I/O2 clock output "L" pulse width | tc (SCLK2)/2-240 | | | ns |
| td(SCLK2-SOUT2) | Serial I/O2 output delay time | | | 0.2 X tc (SCLK2) | ns |
| tv(SCLK2-SOUT2) | Serial I/O2 output valid time | 0 | | | ns |
| tf(SCLK2) | Serial I/O2 clock output falling time | | | 50 | ns |
| tr(CMOS) | CMOS output rising time (Note 2) | | 20 | 50 | ns |
| tf(CMOS) | CMOS output falling time (Note 2) | | 20 | 50 | ns |

Notes1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2: XOUT and XCOUT pins are excluded.

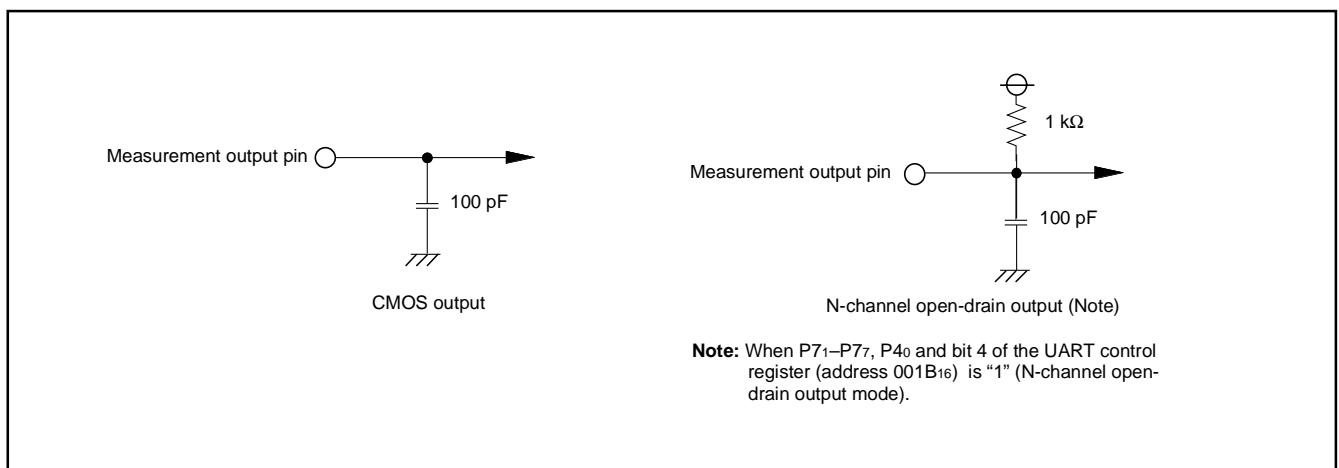


Fig. 69 Circuit for measuring output switching characteristics

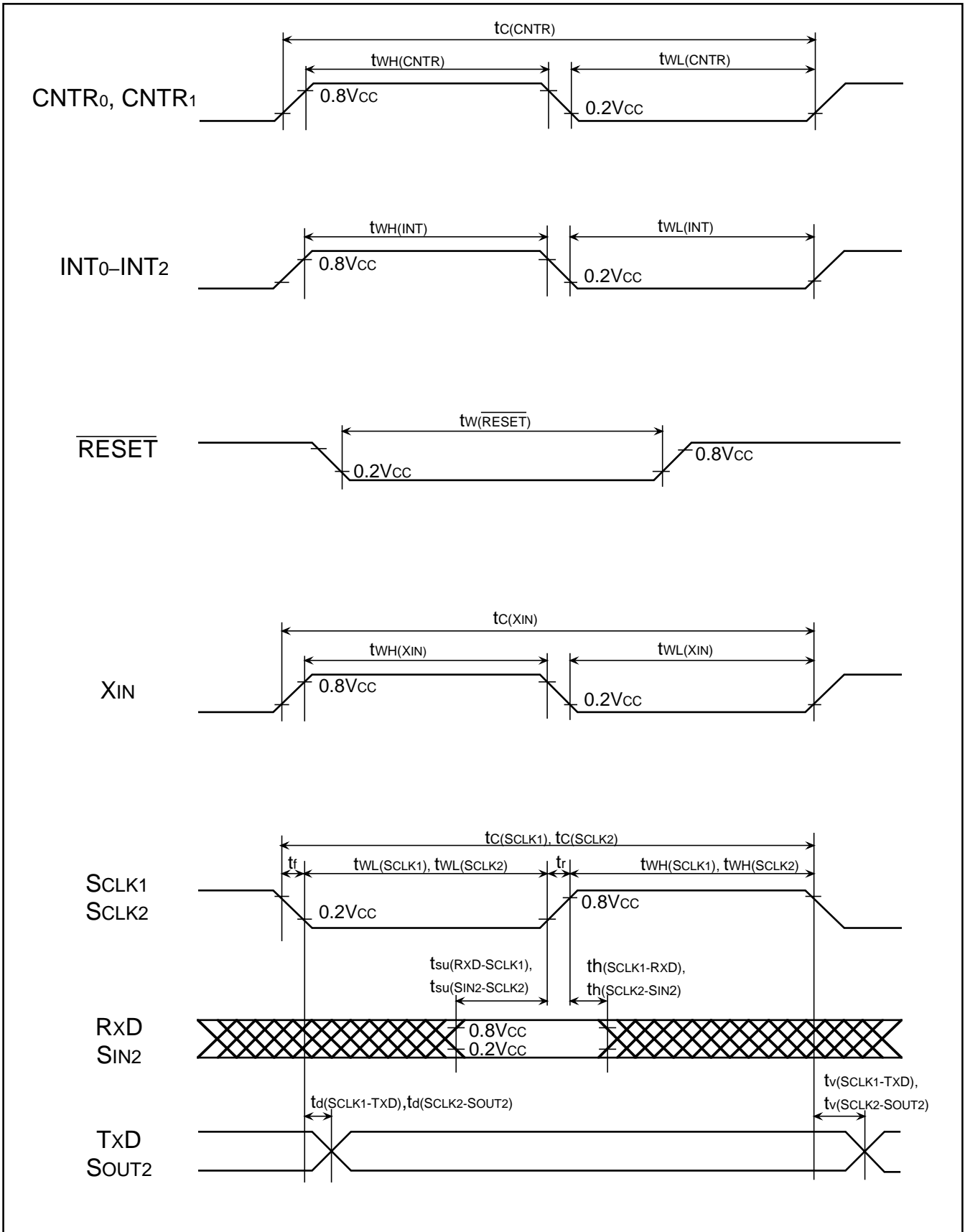


Fig. 70 Timing diagram

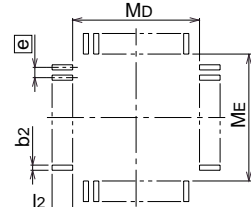
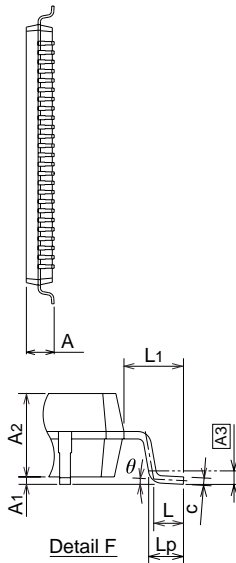
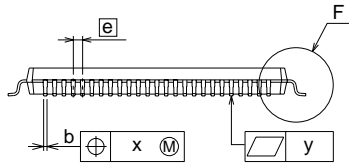
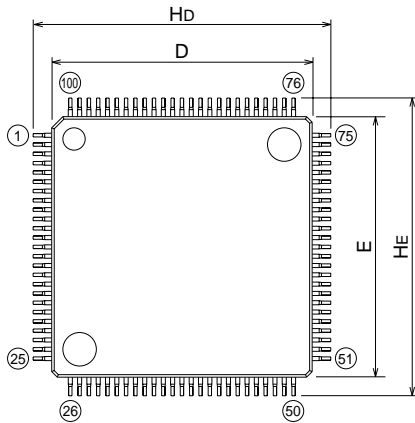
PACKAGE OUTLINE

100P6Q-A

(MMP)

Plastic 100pin 14×14mm body LQFP

| | | | |
|---------------------|------------|-----------|---------------|
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
| LQFP100-P-1414-0.50 | - | 0.63 | Cu Alloy |



Recommended Mount Pad

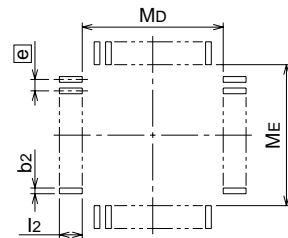
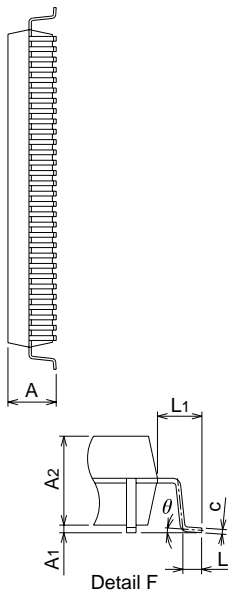
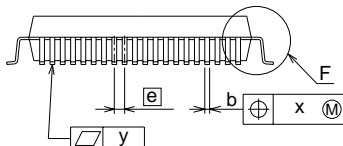
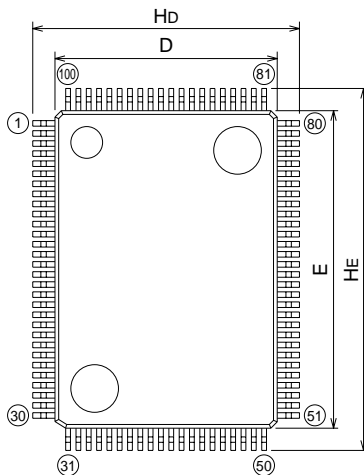
| Symbol | Dimension in Millimeters | | |
|--------|--------------------------|-------|-------|
| | Min | Nom | Max |
| A | - | - | 1.7 |
| A1 | 0 | 0.1 | 0.2 |
| A2 | - | 1.4 | - |
| b | 0.13 | 0.18 | 0.28 |
| c | 0.105 | 0.125 | 0.175 |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| e | - | 0.5 | - |
| Hd | 15.8 | 16.0 | 16.2 |
| HE | 15.8 | 16.0 | 16.2 |
| L | 0.3 | 0.5 | 0.7 |
| L1 | - | 1.0 | - |
| Lp | 0.45 | 0.6 | 0.75 |
| A3 | - | 0.25 | - |
| x | - | - | 0.08 |
| y | - | - | 0.1 |
| θ | 0° | - | 10° |
| b2 | - | 0.225 | - |
| l2 | 0.9 | - | - |
| MD | - | 14.4 | - |
| ME | - | 14.4 | - |

100P6S-A

(MMP)

Plastic 100pin 14×20mm body QFP

| | | | |
|--------------------|------------|-----------|---------------|
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
| QFP100-P-1420-0.65 | - | 1.58 | Alloy 42 |



Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|--------|--------------------------|------|------|
| | Min | Nom | Max |
| A | - | - | 3.05 |
| A1 | 0 | 0.1 | 0.2 |
| A2 | - | 2.8 | - |
| b | 0.25 | 0.3 | 0.4 |
| c | 0.13 | 0.15 | 0.2 |
| D | 13.8 | 14.0 | 14.2 |
| E | 19.8 | 20.0 | 20.2 |
| e | - | 0.65 | - |
| Hd | 16.5 | 16.8 | 17.1 |
| HE | 22.5 | 22.8 | 23.1 |
| L | 0.4 | 0.6 | 0.8 |
| L1 | - | 1.4 | - |
| x | - | - | 0.13 |
| y | - | - | 0.1 |
| θ | 0° | - | 10° |
| b2 | - | 0.35 | - |
| l2 | 1.3 | - | - |
| MD | - | 14.6 | - |
| ME | - | 20.6 | - |

Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

Keep safety first in your circuit designs!

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REVISION HISTORY

7560 GROUP DATA SHEET

| Rev. | Date | Description | |
|------|----------|-------------|---|
| | | Page | Summary |
| 1.0 | 03/28/01 | | First Edition |
| 1.1 | 06/08/01 | 52 | Table 13 VREF Min. VCC+0.3 → VCC |
| 1.2 | 12/05/01 | 1 | <ul style="list-style-type: none"> • A-D converter; 8 bits → 10 bits • Power source voltage; value at EPROM and One Time PROM version and at extended operating temperature version added. • Power dissipation; In high-speed mode: 40 → 32 mW, In low-speed mode: 60 → 45 μW • Operating temperature range; value at extended temperature version added. |
| | | 4 | Table 1; VCC, VSS: voltage valued at EPROM and One Time PROM version and at extended operating temperature version added. |
| | | 6 | Fig. 4; Description about EPROM and One Time PROM version and extended operating temperature version added. |
| | | 7 | Fig. 5; Under development → Mass product |
| | | 8 | GROUP EXPANSION for EPROM and One Time PROM version added. |
| | | 9 | GROUP EXPANSION for extended operating temperature version added. |
| | | 15 | Fig. 12; Reserved area: Note added. Address 0014 ₁₆ : Reserved area → A-D conversion register (ADL). Address 0035 ₁₆ : A-D conversion register (AD) → A-D conversion register (ADH) |
| | | 26 | Fig. 21; P52, P53, P43 revised. |
| | | 38 | [A-D Conversion Register (ADH, ADL)] 0035 ₁₆ , 0014 ₁₆ revised. Comparison Voltage Generator revised. Fig. 38 revised. |
| | | 42 | Voltage Multiplier; 2.1 V → 2.1 V (2.3 V for EPROM and One Time PROM version) |
| | | 49 | Fig. 53; (9) AD conversion register (low-order) added. |
| | | 50 | Oscillation Control; (1) Stop mode revised. |
| | | 54 | DATA REQUIRED FOR MASK ORDERS; URL: mesc → maec ROM PROGRAMMING METHOD added. |
| | | 57 | IOH (avg); (Note 3) added. |
| | | 60 | Table 22; ICC value revised. |
| | | 61 | Table 23; Note added. Conversion time revised. Table 24; A-D converter characteristics at 10-bit A-D mode added. |
| | | 62 | Table 27; tc (CNTR) revised. |
| | | 64 to 77 | ELECTRICAL CHARACTERISTICS (EPROM and One Time PROM version) and ELECTRICAL CHARACTERISTICS (Extended operating temperature version) added. |
| 2.0 | 01/28/03 | 1 | “●Interrupts” of “FEATURES” is partly added. |
| | | 4 | Table 1 is partly revised. |
| | | 5 | Table 2 is partly revised. |
| | | 14 | Figure 11 is partly revised. |

REVISION HISTORY

7560 GROUP DATA SHEET

| Rev. | Date | Description | |
|------|--|-------------|--|
| | | Page | Summary |
| 2.0 | 01/28/03 | 15 | Figure 12 is partly revised. |
| | | 16 | Explanations of "Direcion Registers" of "I/O PORTS" are partly revised. |
| | | 16 | Explanations of "Pull-up Control" of "I/O PORTS" are partly revised. |
| | | 16 | Figure 13 is added. |
| | | 16 | Figure 14 is added. |
| | | 20 | Figure 16 is partly revised. |
| | | 21 | Figure 17 is partly revised. |
| | | 22 | Figure 18 is partly revised. |
| | | 23 | Figure 19 is partly revised. |
| | | 24 | Explanations of "INTERRUPTS" are partly added. |
| | | 25 | Explanations of "■Notes on interrupts" are partly revised. |
| | | 26 | Explanations of "Key Input Interrupt (Key-on Wake Up)" are partly revised. |
| | | 26 | Figure 22 is partly revised. |
| | | 27 | Explanations of "Key Input Interrupt (Key-on Wake Up)" are added. |
| | | 27 | Figure 23 is added. |
| | | 28 | Figure 24 is partly revised. |
| | | 29 | Explanations of "Timer X" are partly added. |
| | | 30 | Explanations of "Timer Y" are partly added. |
| | | 30 | Explanations of "(2) Period measurement mode" of "Timer Y" are partly revised. |
| | | 31 | Explanations of "Timer 1, Timer 2, Timer 3" are partly added. |
| | | 31 | Explanations of "●Timer 2 Write Control" are partly added, |
| | | 32 | Explanations of "(1) Clock Synchronous Serial I/O Mode" are partly added. |
| | | 32 | Note of Figure 29 is partly added. |
| | | 34 | Explanations of "[UART Control Register (UARTON)] are partly revised. |
| | | 36 | Explanations of "Serial I/O2" are partly added. |
| | | 36 | Explanations of "[Serial I/O2 Control Register (SIO2CON)]" are partly added. |
| | | 37 | "●Serial I/O2 Operating" is added. |
| | | 40 | Explanations of "[A-D Control Register (ADCON)]" are partly added. |
| | | 40 | Figure 40 is partly added. |
| | | 41 | Figure 42 is partly added. |
| | | 42 | Figure 44 is partly added. |
| | | 43 | Figure 45 is added. |
| 46 | Explanations of "Voltage Multiplier (3 Times)" are partly revised. | | |
| 50 | Explanation of "Watchdog Timer" are partly revised. | | |
| 51 | Figure 55 is partly revised. | | |
| 52 | Explanations of "RESET CIRCUIT" are partly revised. | | |
| 52 | Figure 56 is partly revised. | | |
| 54 | Explanations of "(2) Wait mode" are partly revised. | | |
| 55 | Figure 61 is partly revised. | | |

REVISION HISTORY

7560 GROUP DATA SHEET

| Rev. | Date | Description | |
|------|----------|---|---|
| | | Page | Summary |
| 2.0 | 01/28/03 | 56 57 57 58, 59 67 67 74 74 81 81 All pages | Figure 62 is partly revised. Explanations of "Interrupt" of "NOTES ON PROGRAMMING" are partly revised. "Timers" of "NOTES ON PROGRAMMING" of Rev. 1.2 is eliminated. "Countermeasures Against Noise" is added. Table 23 is partly revised. Table 24 is partly revised. Table 36 is partly revised. Table 37 is partly revised. Table 49 is partly revised. Table 50 is partly revised. Text expressions are improved. |
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